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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 27/00, 51/20 | A1

(11) International Publication Number: WO 99/54936

(43) International Publication Date: 28 October 1999 (28.10.99)

(21) International Application Number: PCT/GB99/01176

(22) International Filing Date: 16 April 1999 (16.04.99)

(30) Priority Data:
9808061.7 16 April 1998 (16.04.98) GB

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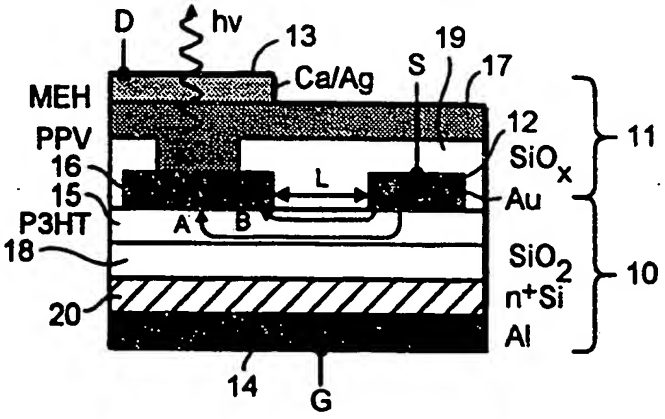
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: POLYMER DEVICES

(57) Abstract

An integrated circuit device comprising: a current drive switching element having an input electrode, an output electrode, a switchable region comprising a semiconductive polymer material electrically coupled between the input electrode and the output electrode, and a control electrode electrically coupled to the switchable region so as to allow the application of a bias to the control electrode to vary the flow of current through the switchable region between the input electrode and the output electrode; and a second circuit element, integrated with the switching element, and electrically coupled with the input electrode of the switching element for receiving a drive current from the switching element.



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POLYMER DEVICES

This invention relates to polymer devices, for instance transistors that comprise a semiconductive polymer material.

There has been extensive work on transistors made with organic materials. Insulated gate field effect transistors (FETs) have been made with polymer semiconductors deposited by solution processing of either the polymer itself or a precursor to form a layer of the final polymer. Figure 1 shows the general structure of such a device. Under the semiconductor polymer layer 1 are two spaced apart metallic electrodes, the drain electrode 2 and the source electrode 3 of the transistor. Below them are a layer 4 of Si/SiO_2 and a metallic gate electrode 5. The device acts as a switch because current flow between the source and drain electrodes is greatly increased when a bias is applied to the gate electrode. One such device, in which the semiconductor polymer is regioregular poly-hexylthiophene (P3HT), is described in more detail in Z. Bao et al., Appl. Phys. Lett. 69, 4108 (1996).

Devices of this type have several problems (see A. R. Brown et al., Science 270, 972 (1995)). First, the through-current from the source to the drain is low because the electronic carrier mobility μ is typically in the range from 10^{-4} to 10^{-6} cm^2/Vs. (See J. H. Burroughes et al., Nature 335, 137 (1988) and A. R. Brown et al., Synthetic Metals 88, 37 (1997)). Most solution-processed polymers have a disordered structure, and it is believed that in these systems the carrier mobility is limited by variable-range hopping between polymer chains. This low mobility rules out such transistors for general current-supply applications. Second, the on-off ratio, i.e. the ratio between the through-current in the on and off states, is poor: less than 10^4 for example. Up to now a polymer transistor with a performance comparable to that of inorganic amorphous silicon transistors has not been demonstrated. As a consequence a preferred approach has been to use molecular (or oligomer) organic materials instead of polymers. Molecular devices

tend to have improved electrical performance but have severe process shortcomings. First, the molecules are generally deposited by vacuum sublimation, typically at substrate temperatures around 100-200°C. This rules out the use of such molecular materials on heat-sensitive substrates. Second, the molecular materials are generally not robust; there are serious concerns about the effect of cracks and microcracks in highly crystalline sublimed molecular films, in particular if deposited on flexible plastic substrates. Third, molecular devices are highly sensitive to subsequent processing steps. Attempts to post-process sublimed molecular films, for example to deposit subsequent layers on top of the sublimed films for multilayer integrated devices, have generally resulted in greatly reduced performance of the buried FETs.

According to a first aspect of the present invention there is provided an integrated circuit device comprising: a current drive switching element having an input electrode, an output electrode, a switchable region comprising a semiconductive polymer material electrically coupled between the input electrode and the output electrode, and a control electrode electrically coupled to the switchable region so as to allow the application of a bias to the control electrode to vary the flow of current through the switchable region between the input electrode and the output electrode; and a second circuit element, integrated with the switching element, and electrically coupled with the output electrode of the switching element for receiving a drive current from the switching element.

According to a second aspect of the present invention there is provided a method for forming an electronic device having a region comprising a semiconductive polymer material, the method comprising depositing the semiconductive polymer by a process which promotes ordering in the deposited polymer. The electronic device according to this aspect of the invention may suitably be a switching element, for example of the type as set out above in relation to the first aspect of the invention.

According to a third aspect of the present invention there is provided an integrated circuit device comprising: a switching element having an input electrode, an output electrode, a switchable region comprising a semiconductive polymer material electrically coupled between the input electrode and the output electrode, and a control electrode electrically coupled to the switchable region so as to allow the application of a bias to the control electrode to vary the flow of current through the switchable region between the input electrode and the output electrode; and an electro-optical circuit element, integrated with the switching element, and electrically coupled to one of the electrodes of the switching element.

The semiconductive polymer may, for instance, be a conjugated polymer (see, for example, PCT/WO90/13148, the contents of which are incorporated herein by reference) or an "intermolecular" semiconducting polymer like poly-vinylcarbazole (PVK) containing short conjugated segments connected by non-conjugated segments.

An insulating layer may be deposited directly or indirectly on top of the electronic device. Preferably this does not substantially degrade the performance of the device. A second circuit element (as in the first aspect of the invention) may also be formed, and is preferably integrated with the said electronic device.

The second circuit element (or the opto-electrical element of the third aspect of the invention) is preferably an element that stores or consumes (preferably significant) electrical energy, e.g. by converting current to an electrical or optoelectrical signal, or an element that converts an optical signal into an electrical signal, e.g. a voltage or a current. The second circuit element is preferably not a switching element. The second circuit element is suitably capable of emitting or detecting light and/or varying the transmission of light through itself. Examples include light-emissive devices, photovoltaic devices and devices such as liquid crystal devices. The device may suitably emit or detect an optical signal, it may be a display device and/or form part of a visual display. The

second circuit element preferably requires a significant drive current for its operation.

Where the second circuit element is a light-emissive element it is preferred that it comprises one or more light-emissive organic materials. The or each light-emissive organic material may be a polymer material, preferably a conjugated or partially conjugated polymer material. Suitable materials include poly-phenylene-vinylene (PPV), poly(2-methoxy-5(2'-ethyl)hexyloxyphenylene-vinylene) (MEH-PPV), PPV-derivatives (e.g. di-alkoxy or di-alkyl derivatives), polyfluorenes and/or co-polymers incorporating polyfluorene segments, PPVs and/or related co-polymers (see, for example, PCT/WO90/13148). Alternative materials include organic molecular light-emitting materials, e.g. tris(8-hydroxyquinoline)aluminium (Alq3) (see, for example, US 4,539,507, the contents of which are incorporated herein by reference), or any other small sublimed molecule or conjugated polymer electroluminescent material as known in the prior art (see, for example, N.C. Greenham and R.H. Friend, Solid State Physics (Academic Press, San Diego, 1995) Vol. 49, pp 1-149). The light emitted by the device may be inside or outside the visible spectral range (400-800 nm). In the latter case materials such as LDS-821 (A. Dodabalapur et al. , IEEE J. Selected Topics in Quantum Electronics 4, 67 (1998)) may be used.

The light-emissive element preferably comprises a cathode for injecting negative charge carriers (electrons) and an anode for injecting positive charge carriers (holes). There is preferably a region (suitably in the form of a layer) of light emissive material (suitably with other layers to improve performance) between the electrodes. The cathode preferably has a work function of less than 3.5eV if a cathode or greater than 4.0eV if a cathode. The material of the cathode is suitably a metal or alloy. Preferred materials include Sm, Yb, Tb, Ca, Ba, Li or alloys of such elements with each other and/or with other metals such as Al. The anode preferably has a work function of greater than 4.0eV and preferably greater than 4.5eV. Preferred materials include conductive oxides (such as ITO and tin oxide) and gold. Preferably one of the electrodes is light-transmissive to allow

light generated in the device to escape. In one preferred configuration the output electrode of the switching element is also one electrode (the anode or the cathode) of the light-emissive element.

The said integrated circuit device is suitably made up of layers. Preferably the switching element is provided by a first layer and the second circuit element is provided by a second layer, so that the two elements are not co-planar. There is suitably an insulating layer between the first layer and the second layer, and there may be electrically conductive interconnects that pass through the insulating layer to electrically connect the switching element and the second circuit element. The terms "first layer" and "second layer" do not imply that the layers are deposited in any specific order: either layer could be deposited first.

There is preferably an insulating layer formed either directly or indirectly on top of the semiconductive polymer. The insulating layer may have a low electrical conductivity. It may be an inorganic dielectric such as SiO_x, MgF or an organic dielectric such as PMMA, polyimide, or poly-vinylphenol (PVP). The insulating layer may be deposited by vacuum deposition techniques or solution processing. It may consist of a composite or a layered structure with several different components of different functionalities. The insulating layer may comprise a material that is capable of attracting residual dopants from the semiconductive polymer. The insulating layer preferably spaces subsequently deposited layers of the second circuit element from the semiconductive polymer. There may be means for electrical interconnection through the insulating layer, such as via holes preferably containing electrically conductive material. The insulating layer may act so as to at least partially encapsulate the semiconductor polymer. The insulating layer is preferably in contact with the semiconductive polymer, most preferably at a location between the input and output electrodes. The insulating layer is suitably of a material that tends to attract dopants such as oxygen from the semiconductive polymer. Oxygen acts as an unintentional dopant for most semiconductive polymers and reduces the ON/OFF current ratio of the switching

element. One possibility is for the insulating layer to be of a silicon oxide, especially a sub-stoichiometric silicon oxide (SiO_x, $x<2$).

Where present, the insulating layer may provide one or more further advantageous features. The insulating layer may have different wetting properties to an adjacent conductive portion of the device (e.g. an electrode) to allow differential wetting effects to be used to guide the deposition of material in a desired location. The wetting properties of the surface of the insulating layer may be engineered to attract or repel subsequently deposited polymer material (suitably solution processable polymer material) and / or to enable the fabrication of a multilayer structure. The insulating layer and / or the electrodes on top of the semiconductive polymer may be used to overcome the solvent compatibility and surface wetting compatibility problems which arise when subsequent layers are deposited. By suitable choice of the insulating layer and its surface properties subsequent layers can be deposited from solvents which would otherwise dissolve or not wet the semiconductive polymer and / or layers underneath. The insulating layer may be capable of attracting dopants such as oxygen to inhibit degradation of the device. The insulating layer may assist in resisting delamination or other forms of mechanical failure due, for example, to differential thermal expansion of the materials on either side of it. The insulating layer may be used to planarize the underlying structure. It may have a composite or layered structure such that the interfaces with the first and second circuit elements may have different and optimum properties such as strong adhesion, or good wetting properties.

The switching element is preferably part of a control circuit for the second circuit element, such as an optical data transmission device or an active matrix control circuit for a light-emissive element in a visual display.

It is preferred that in the finished device the semiconductive polymer material is, at least in part, ordered as between polymer chains. One preferred form of ordering is for the polymer chains and / or the direction of strongest electronic overlap

between adjacent polymer chains (π-π stacking direction) to be predominantly in a plane that also includes a direction generally between the input and output electrodes. The polymer preferably has a conjugated backbone. The ordering may take the form of at least partial phase separation of the polymer. The polymer material is suitably a material that has a tendency to self-organise, preferably when dissolved in a suitable solvent. The polymer suitably has substituents either in or pendent from its backbone which promote ordering of adjacent polymer chains. The polymer may have hydrophobic side-chains. The ordering, whether self-ordering or imposed ordering is preferably into a lamellar structure, most preferably having alternating layers of certain characteristics – for instance alternating conjugated (partially or fully conjugated) and (at least substantially) non-conjugated layers and/or alternating main-chain and side-chain layers. The lamellae are preferentially in a plane that also includes a direction generally between the input and output electrodes.

One preferred form of the semiconductive polymer material is a backbone comprising thiophene groups with alkyl side-chains of a length in the range from C_3 to C_{12}. Poly-hexylthiophene is especially preferred.

More of the components of the device may be of organic materials. One or more (and most preferably all) of the electrodes may comprise an organic material, suitable a conductive material such as polyaniline or poly-ethylene-dioxythiophene, PEDOT doped with polystyrenesulphonic acid (PSS) (Carter et al., Appl. Phys. Lett. 70, 2067 (1997)). One or more (and most preferably all) of the insulating layers contained in the device may be an organic insulator such as polymethylmethacrylate (PMMA) (see G. Horowitz et al., Adv. Mat. 8, 52 (1996)). The whole device structure may be formed on an organic substrate.

The semiconductive polymer is preferably deposited on to a smooth surface. It is therefore preferred that the input and output electrodes are deposited over the semiconductive polymer and/or that the switchable region is in the form of a layer located between the switching electrode and the input and output electrodes.

The step of depositing the semiconductive polymer preferably comprises dissolving the polymer in a solvent in which the polymer has a tendency to self-organise and/or the step of coating the polymer from a solvent in which the polymer has a tendency to self-organise. In either case, the solvent may be chloroform. If the polymer is, for example, poly-hexylthiophene then the concentration of the polymer in the solvent may be in the range from 6 to 20, more preferably 11 to 15 and most preferably around 13mg of polymer in 1ml of solvent. The method of coating is suitably spin-coating, but other processes such as ink-jet printing may be suitable.

The semiconductive polymer is preferably in the form of a layer, and the thickness of the layer is suitably in the range from 200Å to 1000Å, preferably 400Å to 600Å, most preferably around 500Å.

The step of depositing the semiconductive polymer is preferably performed in an inert atmosphere, for example nitrogen or argon.

The step of depositing the semiconductive polymer comprises preparing a substrate which may consist of a sequence of layers to promote the ordering of the polymer and depositing the polymer onto the substrate. This suitably results in preferential alignment of the polymer chains and / or the direction of strongest electronic overlap between adjacent polymer chains (π-π stacking direction) parallel with the surface of the substrate. The step of preparing the substrate comprises making the surface of the substrate more hydrophobic and/or removing water from the surface and/or treating the surface with a silylating agent. The substrate is preferably maintained in an inert atmosphere between such treatment and deposition of the semiconductive polymer.

A method according to the present invention preferably includes the step of integrating an electrooptical device with the electronic device that incorporates the semiconductive polymer. The electrooptical device is suitably formed directly or

indirectly on top of the electronic device, so that the two devices are in a stacked rather than a co-planar arrangement.

Alternative methods of deposition for the polymer/copolymer material(s) include spin-, blade-, meniscus-, dip-coating, self-assembly, ink-jet printing, etc. The polymer material(s) are preferably solution-processible. Layers of small molecule materials can be deposited by vacuum sublimation, etc.

The different layers of the device may be patterned laterally by a suitable technique such as shadow-mask evaporation, ink-jet printing, contact printing, photolithography, etc.

In general, the electronic device is preferably a switching device, more preferably a transistor.

The present invention will now be described by way of example with reference to the accompanying drawings, in which:

figure 2 shows a schematic cross-section of an integrated polymer transistor and polymer light-emissive device;

figure 3 shows the chemical structure of a P3HT polymer chain;

figure 4 shows an idealised ordered P3HT structure;

figure 5 shows the output and transfer characteristics of the integrated transistor of figure 2;

figure 6 shows the performance of the LED and transistor of figure 2 in combination;

figure 7 shows part of a typical active matrix display circuit for current-switching applications;

figure 8 shows a schematic plan view of the layout of a display device having an array of pixels;

figure 9 shows the transconductance in the saturation regime of a typical P3HT FET at 320K and 144K;

figure 10 shows the preferred lamellar ordering of the semiconductive polymer with flexible side chains with the lamellae parallel to the surface of the substrate;

figure 11 shows the improved performance of an LED and transistor in combination as in figure 2 with the MEH-PPV LED replaced by a more efficient F8BT/BFA LED;

figure 12 shows output (top) and transfer (bottom) characteristics of a typical P3HT FET as in figure 1;

figures 13 and 14 show integrated devices with a transistor as the first circuit element and a photovoltaic device (figure 13) or a light-emissive device (figure 14) as the second circuit element.

figures 15 to 18 show examples of schematic structures of integrated devices and

figure 19 and 20 are schematic circuit diagrams for integrated device arrangements.

Figure 2 shows a multi-layer device having an integrated transistor (indicated generally at 10) and light-emissive device (indicated generally at 11). The light-emissive device uses a conjugated polymer material, MEH-PPV, for light emission (D. Braun and A.J. Heeger, Appl. Phys. Lett. 58, 1982 (1991)). The transistor acts to switch the supply of current to the light-emissive device (LED), using a semiconductive layer of P3HT, another conjugated polymer. When a supply voltage is connected between source electrode 12 of the transistor and the cathode 13 of the LED and a bias is applied to the gate electrode 14 of the transistor, current flows from the source 12 through the semiconductor layer 15 of the transistor to the drain electrode 16. The drain 16 also acts as the anode of the LED so the current then flows from the drain 16 and through the light-emissive layer 17 of the LED to the cathode, causing light emission from the layer 17 as indicated at arrow *hv*. Insulating layers 18, 19 of silicon oxide and a layer of n^+-doped silicon 20 lie between the semiconductor layer 15 and the gate 14 and separate the source 12 from the light-emissive layer 17. A device of this type has not previously been feasible because of the low mobilities of typically 10^{-4}-10^{-6}

cm^2/Vs (A. R. Brown et al., Synthetic Metals 88, 37 (1997)) and low through-current performance of prior polymer transistors compared to the relatively high current demands of LEDs, and the difficulties of post processing organic molecular transistors. For example, it has been found that highly crystalline molecular transistors tend to degrade significantly when subsequent layers are deposited on top of the active semiconductor, possibly as a consequence of microcrack formation, whereas polymer transistors have the advantage that they are not typically prone to this mode of failure. As will be described in more detail below, through-currents in the range of 1 to $10mA/cm^2$ have been achieved with the present device, combined with successful post-processing of the transistor. This method of fabricating the transistor, which focuses on the promotion of ordering in the semiconductive polymer(s) results in significantly improved electrical performance compared to prior art devices. The polymer transistors reach mobilities up to $0.1cm^2/Vs$ and ON/OFF current ratios of 10^6-10^8 which is comparable to the performance of inorganic amorphous silicon transistors.

To fabricate the device a wafer is first prepared with a highly doped n^+-Si layer 20 covered by a 2300Å dry thermal SiO_2 gate oxide layer (18) and backed by an aluminium gate electrode 14. The capacitance of the SiO_2 layer 18, C_i, is $15nF/cm^2$.

P3HT for the semiconductor layer 15 is synthesized by the Rieke route (see T. A. Chen et al., J. Am. Chem. Soc. 117, 233 (1995)). P3HT of this type is commercially available from Aldrich. The chemical structure of the P3HT is shown in figure 3. The polymer chain has a conjugated thiophene (25) backbone (indicated generally at 26) and C_6H_{13} alkyl side-chains 27. The polymer is preferably highly regioregular, with head-to-tail coupling *HT* of the hexyl side chains at the 3-position of the thiophene rings suitably greater than 95 %. (Less regioregular polymers could be used).

The P3HT will be spin-coated on to the SiO_2 layer. First, however, steps are taken to improve the ordering of the eventual P3HT layer and the interface of the

P3HT with the SiO_2. The aim is to support the adoption by the P3HT of the structure shown in an idealised form in figure 4 and figure 10, where the side-chains of the P3HT phase segregate, giving short-range order, and where the backbones of P3HT chains lie in the plane of the P3HT layer. The preferred structure is thus of a lamellar-type, with 2-dimensional conjugated layers formed by the backbones and π-π stacking of adjacent chains and separated by layers of phase-segregated side-chains. The structure of the P3HT layer can be investigated using X-ray diffraction. In practice the ordering is unlikely to be complete - there may be localised regions (domains) of short-range order and/or where the chains are in the preferred orientation and other disordered regions. Ordering may not extend through the entire thickness of the P3HT layer: it may for instance be limited to regions near one or both major surfaces. Improvements in device performance have been found to be provided even by limited degrees of ordering; it is not essential for there to be full ordering throughout the P3HT layer.

To promote the formation of an ordered lamellar structure it has been found to be useful to pre-treat the surface of the SiO_2 layer 18 (see figure 4) prior to deposition of the P3HT layer 15. Normally the surface of SiO_2 is terminated with hydroxyl groups, making the surface hydrophilic. A thin layer of water therefore tends to lie over the surface. To encourage the alkyl chains of the P3HT to the surface of the SiO_2 substrate (as shown in figure 4) the surface of the SiO_2 is treated with a silylating agent such as hexamethyldisalazane (HMDS) or alkyl-trichlorosilane to replace the natural hydroxyl groups with alkyl groups (specifically methyl groups). After this treatment to remove the surface water and make the surface of the substrate hydrophobic there is a greater attraction of the P3HT's alkyl chains to the substrate.

An ordered structure in the P3HT layer can also be encouraged by careful choice of the parameters of the P3HT deposition step itself. In certain solvents P3HT tends to aggregate in solution. It has been found that by supporting this tendency to self-organise the ordering of the final P3HT layer can be improved. A stronger concentration of P3HT results in greater self-organisation but (since the solution is

more viscous) a thicker film of P3HT after deposition. Since charge flow through the bulk of the P3HT is believed to have little part in the operation of the final device a thick film of P3HT is not preferred. Therefore, a preferred process for deposition of the P3HT layer is to dissolve P3HT in chloroform ($CHCl_3$) at a concentration of 13mg of P3HT to 1ml of chloroform and spin-coat this solution on to the substrate at a 2000rpm spin speed to yield a film of thickness 500Å. It has also been found to be useful to place the solution on the substrate, to leave it there for some time, e.g. until it appears to start to dry, and then to begin the spin-coating; this appears to further support self-organisation of the P3HT.

Current flow from source to drain through the P3HT layer when a gate voltage is applied is believed to be generally as indicated by arrow A in figure 2. It is believed that one reason why adoption of the structure illustrated in figure 4 may be advantageous is that the best conduction in P3HT is in the direction along the conjugated backbone or by π-π transfer between adjacent chains in the direction out of the general plane of the thiophene groups. It is believed that the P3HT may enhance charge conduction between the source and drain by aligning itself so that (as illustrated in figure 4) the plane containing those directions is parallel or generally parallel with the direction between the source and drain electrodes.

After the P3HT film has been laid down, the source 12 and drain 16 electrodes are deposited by evaporation in high vacuum through a shadow mask at a rate of around 2 to 5Å/s to a thickness of around 500 to 1000Å. The source and drain electrodes are of gold. Other materials and other methods of deposition may, of course be used. The electrodes may help to protect underlying layers, especially from dissolution during deposition of a subsequent polymer layer. The electrodes may help to give more uniform charge carrier injection into adjacent layers.

The layer 19 of sub-stoichiometric silicon oxide (SiO_x, where $x < 2$) is then deposited by thermal evaporation, again through a shadow mask. The mask defines a hole in the layer 19 over the drain electrode 16 which will define the location of the light-emissive region in the finished device. It is helpful to

mechanically align the source/drain shadow mask and the shadow mask for the layer 19 to ensure correct location of the hole over the drain electrode. The insulating layer of SiO_x has different wetting properties than the conducting Au electrode regions and the semiconductive polymer. The insulating layer and its wetting properties are used to enable the deposition of a continuous subsequent layer of the light-emissive material from solution. It may also be used to direct the deposition of the light-emissive layer into desired locations.

A layer 17 of methoxy-5-(2'-ethyl-hexyloxy)-p-phenylene vinylene (MEH-PPV) is then spin-coated on top of the layer 19 and the device is completed by evaporation of a semi-transparent Ca/Ag cathode 13 of thickness 20nm.

The fact that no photolithography is needed in fabricating the device has clear advantages.

Performing the process steps in an inert atmosphere such as nitrogen or argon has been found to be advantageous. Air and water tend to degrade the surface of the SiO_2 layer 18, as described above, and also seem to dope the P3HT. Therefore, it is preferable to store the P3HT in an inert atmosphere before use; to make up the P3HT solution in an inert atmosphere and to perform the spin-coating in an inert atmosphere. It should be noted, however, that once the device has been fabricated the P3HT is to some extent environmentally protected by being sandwiched between the silicon oxide layers 18 and 19. This is a significant advantage of the present device. Indeed, it is believed that the sub-stoichiometric SiO_x layer 19 may act as an oxygen getter to reduce doping near the upper surface of the P3HT. This is important because current flow at that surface of the P3HT is believed to contribute to charge leakage from the source to the drain when the transistor is in its off state. (See arrow B in figure 2). Reduction of doping there may therefore improve the on-off ratio of the transistor. The gettering effect of the SiO_x layer 19 may be further enhanced by providing a hydrophilic layer over the P3HT layer. The bulk doping of the final P3HT layer

may be around $5x10^{15}cm^{-3}$. (This can be estimated from capacitance-voltage measurements).

Figure 5 shows the output and transfer characteristics of the transistor portion of an example of the present device where the channel length (L in figure 2) is 155μm, the channel width (W) is 1500μm and the source-drain voltage (V_{sd}) is -80V. (Clearly, much smaller devices than this could be made, and further performance improvements would be expected). Figure 5 shows that the transistor switches on at around V_0 = 0 to 4V with sharp turn-on characteristics with subthreshold slopes of 1 to 1.5V/decade. The on/off ratio between V_g ~ 0V and V_g = -60V exceeds 10^6, which represents an improvement by more than two orders of magnitude over the performance noted in the paper by Z. Bao et al. cited above. The off current is believed to be limited by gate leakage through the oxide layer 18. These figures show that the performance of the present transistor device is comparable with conventional amorphous silicon (a-Si) devices (see C. C. Wu et al., IEEE Electron Device Letters 18, 609 (1997)). From the transfer characteristics in the saturation regime mobilities of μ_{FET}^{sat} = 0.05 to 0.1cm^2/Vs can be extracted. This is also a significant improvement over the prior art. Bulk conductivity is also reduced and is estimated to be less than 10^{-8}S/cm.

Figure 6 illustrates the performance of the light emitting device in combination with the transistor, showing brightness of the LED (triangles) and drain current supplied by the FET to the LED (circles) as a function of FET gate voltage, with V_{sd} = -70V. The device used had an LED area of 300μm x 430μm and L = 75μm, W = 1500μm. At V_g = -50V the FET supplies a current density of ~10mA/cm^2 to the LED, resulting in a brightness of the order of 1 to 5cd/m^2. The insert in figure 6 shows the (linear) relationship between the drain current (I_d) and the photocurrent (I_p) detected by a Si photodiode mounted above the LED. From this the external quantum efficiency of the LED can be estimated to be of the order of η_{exc} = 0.01%. More efficient light-emitting devices could be made using well-known techniques such as providing charge transport layers, e.g. of polystyrene sulphonic acid doped polyethylene dioxythiophene (PEDOT-PSS), between one

or both of the LED electrodes 13, 16 and the light-emissive layer; using another emissive material instead of MEH-PPV, or a blend of materials; or using different materials for the electrodes. (See D. Braun and A. Heeger, Appl. Phys. Lett. 58, 1983 (1991); and N.C. Greenham and R.H. Friend, Solid State Physics (Academic Press, San Diego, 1995) Vol. 49, pp 1-149). As is shown below with an LED with external quantum efficiency of 1% the current density of $10mA/cm^2$ is sufficient for video-brightness displays of $100Cd/m^2$.

As an example for an optical data transmission element in which the device could be used figure 7 shows the usual circuit for controlling a pixel of an active matrix LED display (see, for example, US 5,550,066, the contents of which are incorporated herein by reference), where line 30 is the current supply line, lines 31a and 31b are the row and column lines, transistor 32 is the switching transistor, capacitor 33 is the storage capacitor, transistor 34 is the current transistor and 35 indicates the light-emissive pixel itself. The integrated LED and transistor of figure 2 could embody the pixel 35 and the transistor 34, enclosed by the dashed line at 36 in figure 7. This represents an especially convenient embodiment of such an active matrix circuit. Figure 8 shows a plan view of one layout that could be used in a multi-pixel display, with the current supply line 30 running beside a row of pixels 35 and connecting the source electrodes 12 (shown at 37 in figure 7) of those pixels' transistors together. The gates 14 (shown at 38 in figure 7) of the transistors could be supplied from below or from other circuitry on the same plane. The transistors 32 could be provided by other transistors of the type described above and the capacitor 33 could be provided by an organic or inorganic dielectric layer.

Alternative materials could be used in all the layers of the device of figure 2. Instead of P3HT similar polymers with longer or shorter alkyl side-chains or other semiconductive polymers with a tendency to self-organise could be used, such as poly-thienylenevinylenes (PTV) (A. R. Brown et al., Science 270, 972 (1995)), poly-paraphenylenes (PPP) (G. Klärner et al., Synth. Met. 84, 297 (1997)), poly-diacetylenes (K. Donovan, et al. Phil. Mag. B 44, 9 (1981)) or liquid crystalline

molecules and polymers. One preferred approach may be to use polymers for all the layers, replacing the metal electrodes with a conductive polymer such as polyaniline and the silicon oxides with, for example, polymethylmethacrylate (PMMA) (see G. Horowitz et al., Adv. Mat. 8, 52 (1996)). An all-polymer device of this type has clear process advantages in fabrication.

It may be advantageous for the lamellar structure to generally take the form of alternating layers of conjugated and non-conjugated regions of polymers.

Poly-3-hexylthiophene is an example of a conjugated polymer with a rigid-rod conjugated backbone and flexible side chains. The latter make the polymer soluble in common organic solvents. However, the side chains are often electrically insulating.

Like most other rigid-rod polymers with flexible side chains such as poly-dialkoxy-p-phenylene-vinylene (S.-A. Chen, E.-C. Chang, Macromoelcules 31, 4899 (1998)), poly-alkyl-diacetylenes, or poly-phenylene-terephthalates (for a review see D. Neher, Adv. Mat. 7, 691 (1995)) poly-3-alkylthiophenes adopt a lamellar-type structure in the solid state. Two-dimensional (2D) conjugated planes are formed by the conjugated backbones and π-π interchain stacking between adjacent chains. The conjugated planes are separated by layers of insulating side chains. High charge carrier mobilities in FET devices are obtained if the conjugated lamellae are oriented parallel to the plane of the film. If the polymer has no preferential orientation or if the layers are oriented normal to the film mobilities are by more than two orders of magnitude smaller. This is thought to be because in the parallel orientation charge carriers can easily move from chain to chain along the direction of π-π interchain stacking without being hindered by the insulating side chains. Therefore, a lamellar structure with parallel orientation of the conjugated layers is most likely to yield high mobilities in rigid-rod conjugated polymers with flexible side chains. Other polymers that may exhibit such behaviour include polyfluorenes such as poly-(2,7-(9,9-di-*n*-octylfluorene)-3,6-benzothiadiazole) ("F8BT").

Since the general current flow in the transistor is in the direction of arrow A in figure 2 it may be advantageous to promote alignment of the P3HT chains in that direction, for example by depositing the P3HT onto a substrate with a preferred linear orientation induced by mechanical rubbing, photoalignment (M. Schadt et al., Nature 381, 212 (1996)) etc., in addition to promoting ordering in the direction normal to the plane of the P3HT layer.

It is believed that the improved performance of the transistor described herein may be due to the formation of extended current transporting states. For these states to be formed there would be expected to be pronounced short-range, if not microcrystalline order. The ordered lamellar structure of the P3HT may result in an electronic structure with extended states due to the self-organised, short-range order and localised states associated with grain boundaries, aggregates, conformational defects, residual doping, etc. It may be that the Fermi level (E_F) enters the distribution of localised states, as would for example be the case with a relatively broad distribution with small density of states, so that μ_{FET} would show a strong dependence on the gate voltage V_g. Figure 9 shows the transconductance in the saturation regime of a P3HT FET at 320K and 144K.

It should be noted that the use of the top source and drain contacts (as shown in figure 2) rather than bottom contacts (as shown in figure 1) is believed to help to ordering of the P3HT by allowing a smooth surface for the P3HT to be deposited upon. However, bottom electrodes (or other electrode configurations) could be used.

The use of polymer conjugated materials (such as P3HT) rather than oligomer / small molecule materials also provides some process advantages. Polymer materials can generally be deposited at room temperature, making processing easier and cheaper and affording compatibility with a wider range of substrate materials (e.g. plastics instead of glass for a display device). Polymers are also generally more robust and less prone to damage during post-processing steps.

Another advantage of polymer devices, especially over inorganic devices, is that polymer layers are generally flexible. This can reduce problems of mismatch between successive layers, making multi-layer integration easier.

Instead of supplying an organic LED as shown above, the transistor of figure 2 could be used as part of any compatible integrated circuit, used to supply an optoelectrical device to emit an optical signal, or to supply an inorganic LED or another type of display device such as a liquid crystal pixel or a memory element, a logic element or another polymer transistor. The device's improved through-current makes it especially suitable for supplying circuit element(s) that use significant currents (for instance to perform a function such as emitting light or for the purpose of charge storage) rather than (or in addition to) merely switching.

The SiO_x layer 19 could be omitted, relying on the area of overlap of the electrodes 13 and 16 to define the light-emissive region of the device. In fabricating the device it would then be important to ensure solvent compatibility with the material of layer 15 during deposition of the layer 17. Avoiding this difficulty is another advantage of the layer 19.

The performance of FET-LED could be improved by replacing the single layer MEH-PPV described above with a double-layer LED using a hole transporting layer of poly (2,7-(9,9-di-n-octylfluorene) - (1,4-phenylene - ((3-carboxyphenyl) imino) -1,4-phenylene- ((3-carboxyphenyl)imino)-1,4-phenylene)) (BFA) and a light-emissive polymer layer of F8BT. With such a double-layer LED practical video brightnesses in excess of 100 Cd/m^2 have been obtained (See figure 11).

P3HT FETs with field-effect mobilities of 0.05-0.1 cm^2/Vs and ON-OFF current ratio of 10^6-10^8 have been fabricated. To obtain high ON-OFF current ratio the processing is performed under inert N_2 atmosphere and residual doping atoms are reduced chemically, for example by evaporating a layer of substoichiometric SiO_x onto the surface of the P3HT or by exposing the films to reducing hydrazine

vapour for a few minutes. The characteristics of such a device are shown in figure 12. They are comparable to those of a-Si thin-film transistors.

Instead of transmitting an optical signal from the second circuit element (for example, an LED) by supplying a drive current to it from the first circuit element (FET), one may also detect an optical signal with the second circuit element and convert it into a current or voltage signal with the first circuit element. One possible implementation of such a function is shown in figure 13, in which the second circuit element is a polymer photodiode operating in either the photovoltaic or photocurrent mode sandwiched between a cathode and the floating gate electrode of a polymer transistor. When the photodiode absorbs light a photovoltage is developed on the gate electrode of the transistor resulting in a modulation of the transistor source-drain current. The configuration of this integrated photodiode-FET device is analogous to that of the LED-FET device (shown for comparison in figure 14). It could be the first stage of a circuit to amplify the signal from the photodiode for further processing in a logic circuit.

In figures 13 to 18 the components of the illustrated devices are indicated by the following reference numerals: substrate 50, drain electrode 51, source electrode 52, transistor active region 53, gate insulator layer 54, insulator layer 55, gate electrode 56, light-emissive/light-sensitive region 57, electrode 58, light direction arrow 59, switching current flow arrow 60.

The active layer 57 of the polymer photodiode of figure 13 comprises a photoconductive polymer or a blend of photoconductive polymers in a single or multilayer configuration. Possible examples are blends of poly-octyl-thiophene (P3OT) or P3HT with methoxy-5-(2'-ethyl-hexyloxy)-cyano-phenylene-vinylene (MEH-CN-PPV) (see M. Granström, K. Petritsch, A.C. Arias, A. Lux, M.R. Andersson, R.H. Friend, Nature 395, 257 (1998); J.J.M. Halls et al., Nature 376, 498 (1995)).

The transmitter and receiver devices described above may be used together to form integrated optoelectronic circuits in which an optical signal is detected, and converted into another optical signal according to a specified logic function. The logic function may be executed by an integrated logic circuit with transistors as key elements (C.J. Drury et al., Appl. Phys. Lett. 73, 108 (1998)). This is illustrated schematically in figure 19. The wavelength of the incoming and outgoing signals may be the same or different. Either or both of them may be outside the spectrum visible to the human eye. The device may be realised on a common substrate by integrating the detecting, transmitting and electronic components. The electrical power required to operate such a circuit may be provided by a photovoltaic cell (J.J.M. Halls et al., Nature 376, 498 (1995)) or a thin-film battery (A. G. Mac Diarmid, R. B. Kaner, in "Handbook of Conducting Polymers", ed. T.A. Skotheim, Vol. 1, p. 689 (Marcel Dekker, New York, 1986) integrated onto the same substrate. Some or all of the components of the integrated optoelectronic circuit may be organic. Some or all of the components may be polymers which can be processed from solution and patterned by suitable techniques such as ink-jet printing.

The transmitter and receiver devices may also be fabricated on separate substrates. A light signal may be used to transmit data between the two devices. This is illustrated schematically in figure 20.

A light transmitter and receiver may be integrated as first and second circuit elements in different configurations. The second circuit element may either be on top of the first element (figure 15), below the first element (figure 16) or next to the first element (figure 17). Figures 15 to 17 show example configurations. The light may be emitted through the top/or bottom electrode. The electrodes of the LED may be semitransparent (for example, thin metal films) or transparent (such as indium-tin-oxide conductors).

The light may also be coupled into a waveguide (figure 18). To provide waveguiding the usual refractive index relationships must be observed: in this

case $n_2 > n_1$ (air), n_3 (SiO_x), n_4 (P3HT). This can be used to channel towards external internal ports which have optical/electrical functionality. To couple the light into the transistor or other elements in a lower or upper level the refractive index contrast may be suitably reduced or reversed so as to allow coupling through leaky waveguide modes or the tail of a truly guided mode.

One or more of the layers of the device may include nanoparticles to enhance their operation.

The present invention may include any feature or combination of features disclosed herein either implicitly or explicitly or any generalisation thereof irrespective of whether it relates to the presently claimed invention. In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention.

CLAIMS

1. An integrated circuit device comprising:

a current drive switching element having an input electrode, an output electrode, a switchable region comprising a semiconductive polymer material electrically coupled between the input electrode and the output electrode, and a control electrode electrically coupled to the switchable region so as to allow the application of a bias to the control electrode to vary the flow of current through the switchable region between the input electrode and the output electrode; and

a second circuit element, integrated with the switching element, and electrically coupled with the output electrode of the switching element for receiving a drive current from the switching element.

2. An integrated circuit device as claimed in claim 1, wherein the integrated circuit device is made up of layers, the switching element being provided by a first layer and the second circuit element being provided by a second layer.

3. An integrated circuit device as claimed in claim 2, comprising an insulating layer between the first layer and the second layer.

4. An integrated circuit device as claimed in claim 3, comprising electrically conductive interconnects that pass through the insulating layer to electrically connect the switching element and the second circuit element.

5. An integrated circuit device as claimed in any of claims 1 to 4, wherein the second circuit element is a display element.

6. An integrated circuit device as claimed in claim 1 to 5, wherein the second circuit element is a light-emissive element.

7. An integrated circuit device as claimed in claim 6, wherein the light-emissive element comprises a light-emissive organic material.

8. An integrated circuit device as claimed in claim 7, wherein the light-emissive organic material is a light-emissive polymer material.

9. An integrated circuit device as claimed in any of claims 6 to 8, wherein the output electrode of the switching element is one electrode of the light-emissive element.

10. An integrated circuit device as claimed in any of claims 5 to 9, wherein the switching element is part of an active matrix control circuit for the display element.

11. An integrated circuit device as claimed in any preceding claim, wherein, at least in part, the semiconductive polymer material is ordered as between polymer chains.

12. An integrated circuit device as claimed in any preceding claim, wherein, at least in part, the semiconductive polymer material is phase-separated.

13. An integrated circuit device as claimed in any preceding claim, wherein the semiconductive polymer material is a material that has a tendency to self-organise.

14. An integrated circuit device as claimed in claim 13, wherein the semiconductive polymer material is a material that has a tendency to self-organise in a lamellar structure.

15. An integrated circuit device as claimed in claim 14, wherein the semiconductive polymer material is a material that has a tendency to self-organise in a lamellar structure in which layers of conjugated regions alternate with layers of non-conjugated regions.

16. An integrated circuit device as claimed in any preceding claim, wherein the semiconductive polymer has a conjugated backbone.

17. An integrated circuit device as claimed in any preceding claim, wherein the semiconductive polymer has substituents either in or pendent from its backbone which promote ordering of adjacent polymer chains.

18. An integrated circuit device as claimed in any preceding claim, wherein the semiconductive polymer has hydrophobic side-chains.

19. An integrated circuit device as claimed in any preceding claim, wherein the semiconductive polymer is poly-hexylthiophene.

20. An integrated circuit device as claimed in any preceding claim, wherein at least one of the input, output and switching electrodes comprises an organic material.

21. An integrated circuit device as claimed in any of claims 4 to 20 as dependant directly or indirectly on claim 3, wherein the insulating layer comprises an organic material.

22. An integrated circuit device as claimed in any preceding claim, wherein the switchable region is in the form of a layer located between the switching electrode and the input and output electrodes.

23. A method for forming an electronic device having a region comprising a semiconductive polymer material, the method comprising depositing the semiconductive polymer by a process which promotes ordering in the deposited polymer.

24. A method as claimed in claim 23, wherein the step of depositing the semiconductive polymer comprises dissolving the polymer in a solvent in which the polymer has a tendency to self-organise.

25. A method as claimed in claim 23 or 24, wherein the step of depositing the semiconductive polymer comprises coating the polymer from a solvent in which the polymer has a tendency to self-organise.

26. A method as claimed in any of claims 23 to 25, wherein the step of depositing the semiconductive polymer is performed in an inert atmosphere.

27. A method as claimed in any of claims 23 to 26, wherein the step of depositing the semiconductive polymer comprises preparing a substrate to promote the ordering of the polymer and depositing the polymer onto the substrate.

28. A method as claimed in claim 27, wherein the step of preparing the substrate comprises making the surface of the substrate more hydrophobic.

29. A method as claimed in any of claims 23 to 28, wherein the method comprises depositing at least one electrode over the semiconductive polymer.

30. A method as claimed in any of claims 23 to 29, wherein the polymer is a material that has a tendency to self-organise.

31. A method as claimed in any of claims 23 to 29, wherein the polymer has a conjugated backbone.

32. A method as claimed in any of claims 23 to 31, wherein the polymer has substituents either in or pendent from its backbone which promote ordering of adjacent polymer chains.

33. A method as claimed in any of claims 23 to 32, wherein the polymer has hydrophobic side-chains.

34. A method as claimed in any of claims 23 to 33, wherein the polymer is poly-hexylthiophene.

35. A method as claimed in any of claims 23 to 34, further comprising the step of forming a light-emissive device over the electronic device.

36. A method as claimed in claim 35, wherein the light-emissive device is integrated with the electronic device.

37. A method as claimed in claim 34 or 36, wherein the light-emissive device comprises a light-emissive organic material.

38. A method as claimed in any of claims 23 to 37, wherein the electronic device is a switching device.

39. A method as claimed in claim 38, wherein the electronic device is a transistor.

40. A method as claimed in claim 38 or 39, wherein the electronic device comprises an input electrode, an output electrode, a switchable region electrically coupled between the input electrode and the output electrode and which comprises the semiconductive polymer material, and a control electrode electrically coupled to the switchable region so as to allow the application of a bias to the control electrode to vary the flow of current through the switchable region between the input electrode and the output electrode.

41. A method as claimed in any of claims 23 to 40, wherein the wetting properties of the surface of the first circuit element are engineered to enable the deposition of subsequent layers on top of it.

42. A method as claimed in any of claims 23 to 41, further comprising the step of forming an insulating layer on top of the semiconductive polymer.

43. A method as claimed in claim 42, wherein the insulating layer is of a material that is capable of attracting residual dopants from the semiconductive polymer.

44. A method as claimed in claim 41 to 43, wherein the wetting properties of the surface of the insulating layer are engineered to enable the deposition of another layer on top of it.

45. A method as claimed in claim 41 to 44, wherein different wetting properties of the surface of the insulating layer and that of adjacent conductive regions are used to guide the deposition of subsequent layers into a desired location.

46. A method as claimed in claim 41 to 45, wherein the insulating layer is used to avoid dissolving and degradation of the layers of the first circuit element during the deposition or operation of the layers of the second circuit element.

47. A method as claimed in claim 41 to 46, wherein the mechanical properties of the insulating layer resist delamination of the device or other types of mechanical failure.

48. A method as claimed in claim 23 to 47, wherein a conducting layer between the first and second circuit element is deposited to ensure electrical compatibility between the two elements.

49. A method as claimed in claim 23 to 48, wherein the conducting layer ensures uniform current injection into the second circuit element.

50. A method as claimed in claim 23 to 49, wherein the conducting layer ensures efficient carrier injection into the second circuit element.

51. An integrated circuit device comprising:

a switching element having an input electrode, an output electrode, a switchable region comprising a semiconductive polymer material electrically coupled between the input electrode and the output electrode, and a control electrode electrically coupled to the switchable region so as to allow the application of a bias to the control electrode to vary the flow of current through the switchable region between the input electrode and the output electrode; and

an electro-optical circuit element, integrated with the switching element, and electrically coupled to an electrode of the switching element.

52. An integrated circuit device as claimed in claim 51, wherein the integrated circuit device is made up of layers, the switching element being provided by a first layer and the electro-optical circuit element being provided by a second layer.

53. An integrated circuit device comprising:

a switching element having an input electrode, an output electrode, a switchable region comprising a semiconductive polymer material electrically coupled between the input electrode and the output electrode, and a control electrode electrically coupled to the switchable region so as to allow the application of a bias to the control electrode to vary the flow of current through the switchable region between the input electrode and the output electrode; and

a second circuit element, integrated with the switching element in a multilayer-stack configuration, and electrically coupled to an electrode of the switching element.

54. An integrated circuit device as claimed in claim 53, in which the second circuit element is also switching element.

55. An integrated circuit device as claimed in claim 52 to 54, comprising an insulating layer between the first layer and the second layer.

56. An integrated circuit device as claimed in claim 55, comprising electrically conductive interconnects that pass through the insulating layer to electrically connect the switching element and the electro-optical circuit element.

57. An integrated circuit device as claimed in any of claims 51 to 53 and 55 to 56, wherein the second circuit element is a light-emissive element.

58. An integrated circuit device as claimed in claim 57, wherein an input electrode of the electro-optical circuit element is electrically coupled to an output electrode of the switching element.

59. An integrated circuit device as claimed in any of claims 51 to 53 and 55 to 56, wherein the second circuit element is a light-sensitive element.

60. An integrated circuit device as claimed in claim 59, wherein an output electrode of the light-sensitive element is electrically coupled to an input electrode of the switching element.

61. An integrated circuit device as claimed in claim 59, wherein an output electrode of the light-sensitive element is electrically coupled to the control electrode of the switching element.

62. An integrated circuit device as claimed in any of claims 51 to 53 and 55 to 61, wherein the opto-electrical element has an opto-electrically active region comprising a light-emissive and/or light-sensitive organic material.

63. An integrated circuit device as claimed in claim 62, wherein the light-emissive and/or light-sensitive organic material is a polymer material.

64. An integrated circuit device as claimed in any of claims 51 to 63, wherein, at least in part, the semiconductive polymer material is ordered as between polymer chains.

65. An integrated circuit device as claimed in any of claims 51 to 64, wherein, at least in part, the semiconductive polymer material is phase-separated.

66. An integrated circuit device as claimed in any of wherein claims 51 to 65, wherein the semiconductive polymer material is a material that has a tendency to self-organise.

67. An integrated circuit device as claimed in claim 66, wherein the semiconductive polymer material is a material that has a tendency to self-organise in a lamellar structure.

68. An integrated circuit device as claimed in claim 67, wherein the semiconductive polymer material is a material that has a tendency to self-organise in a lamellar structure in which layers of conjugated regions alternate with layers of non-conjugated regions.

69. An integrated circuit device as claimed in any of claims 51 to 68, wherein the semiconductive polymer has a conjugated backbone.

70. An integrated circuit device as claimed in any of claims 51 to 68, wherein the semiconductive polymer has substituents either in or pendent from its backbone which promote ordering of adjacent polymer chains.

71. An integrated circuit device as claimed in any of claims 51 to 70, wherein the semiconductive polymer has hydrophobic side-chains.

72. An integrated circuit device as claimed in any of claims 51 to 71, wherein the semiconductive polymer is poly-hexylthiophene.

73. An integrated circuit device as claimed in any of claims 51 to 72, wherein at least one of the input, output and switching electrodes comprises an organic material.

74. An integrated circuit device as claimed in any of claims 51 to 73 as dependant directly or indirectly on claim 54, wherein the insulating layer comprises an organic material.

75. An integrated circuit device as claimed in any of the above claims which forms part of a larger circuit which may comprise any or all of the following items: switching elements, resistive elements, capacitive elements, photovoltaic elements, photoconductive elements, light emissive elements, and or energy storage devices.

76. A method for forming an electronic device, substantially as herein described with reference to figures 2 to 20 of the accompanying drawings.

77. An electronic device formed by a method according to any of claims 23 to 50 or 76.

78. An electronic device substantially as herein described with reference to figures 2 to 20 of the accompanying drawings.

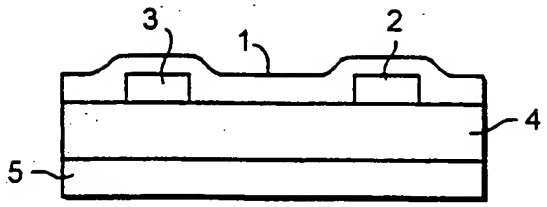

FIG.1

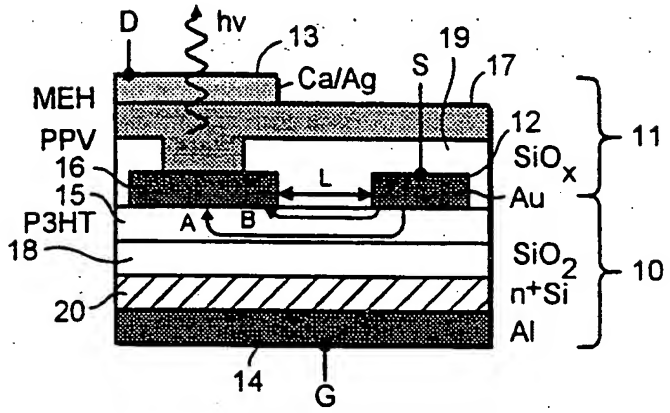

FIG. 2

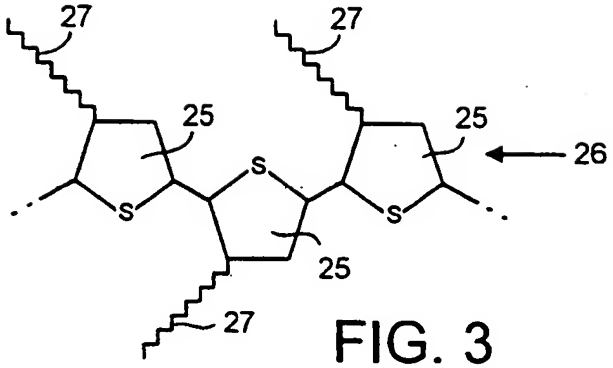

FIG. 3

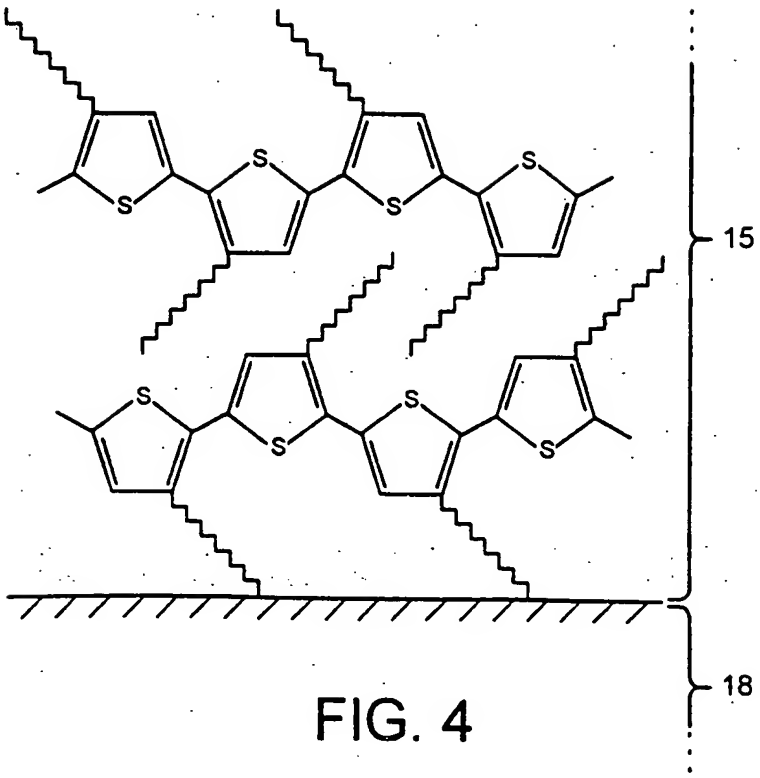
S
15
18

FIG. 4

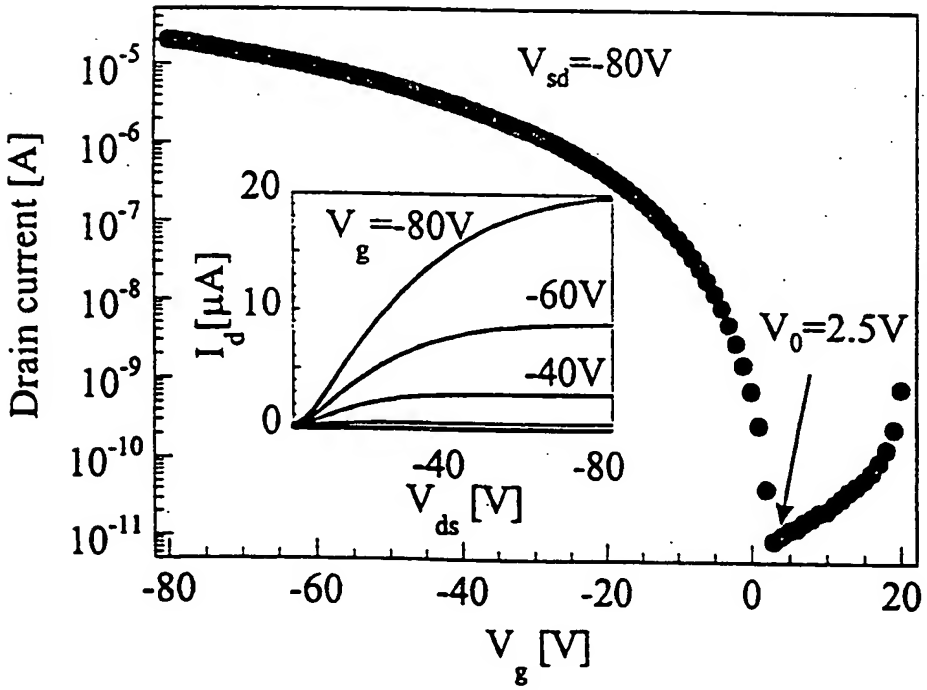
V_{sd}=-80V
V_0=2.5V
Drain current [A]
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
-80
-60
-40
-20
0
20
V_g [V]
I_d[μA]
20
10
0
V_g =-80V
-60V
-40V
-40
-80
V_{ds} [V]

FIG. 5

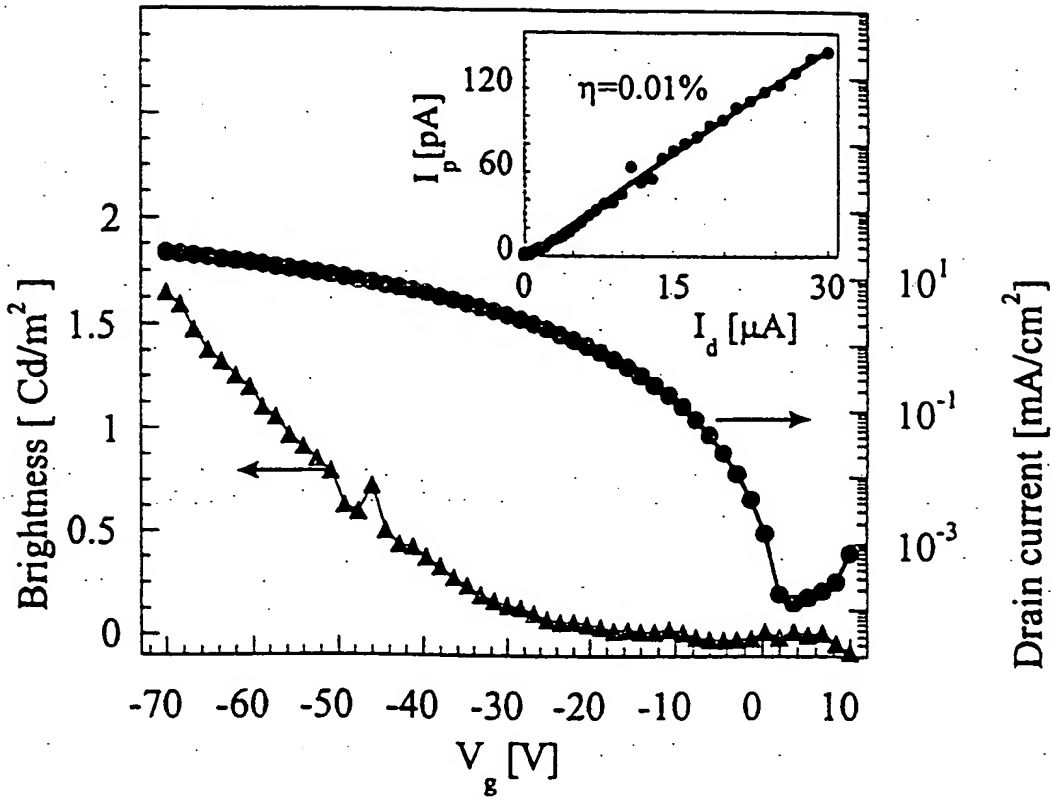
Brightness [Cd/m^2]
Drain current [mA/cm^2]
V_g [V]
I_d [μA]
I_p [pA]
η=0.01%
2
1.5
1
0.5
0
-70 -60 -50 -40 -30 -20 -10 0 10
10^1
10^{-1}
10^{-3}
120
60
0
0 15 30

FIG. 6

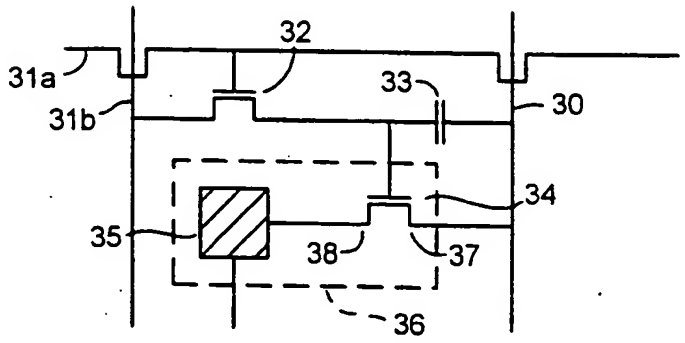
32
31a
31b
33
30
34
35
38
37
36

FIG. 7

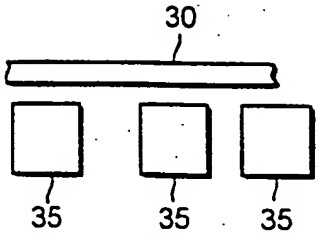
30
35
35
35

FIG. 8

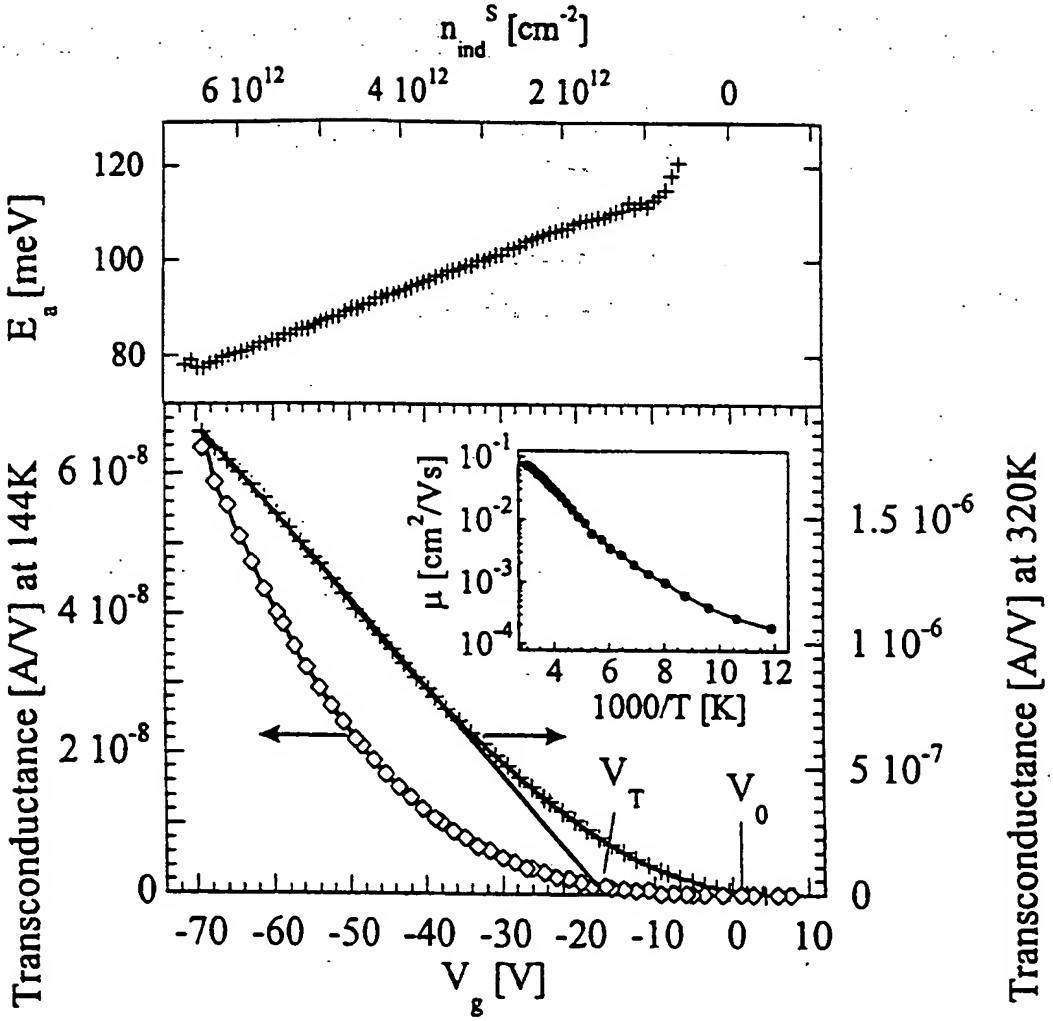
n ind S [cm-2]
6 10^12
4 10^12
2 10^12
0
E a [meV]
120
100
80
Transconductance [A/V] at 144K
6 10^-8
4 10^-8
2 10^-8
0
μ [cm2/Vs]
10^-1
10^-2
10^-3
10^-4
4 6 8 10 12
1000/T [K]
V T
V 0
-70 -60 -50 -40 -30 -20 -10 0 10
V g [V]
1.5 10^-6
1 10^-6
5 10^-7
0
Transconductance [A/V] at 320K

FIG. 9

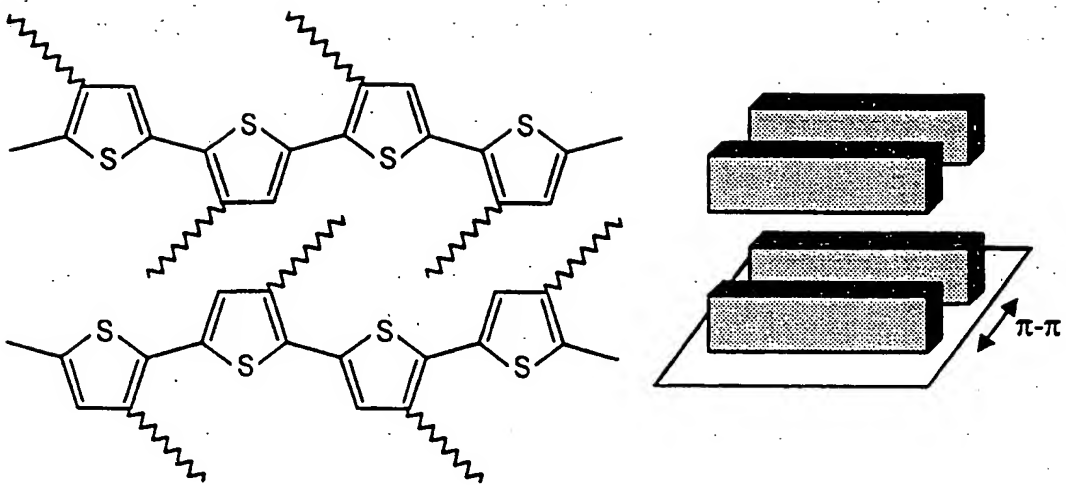

FIG. 10

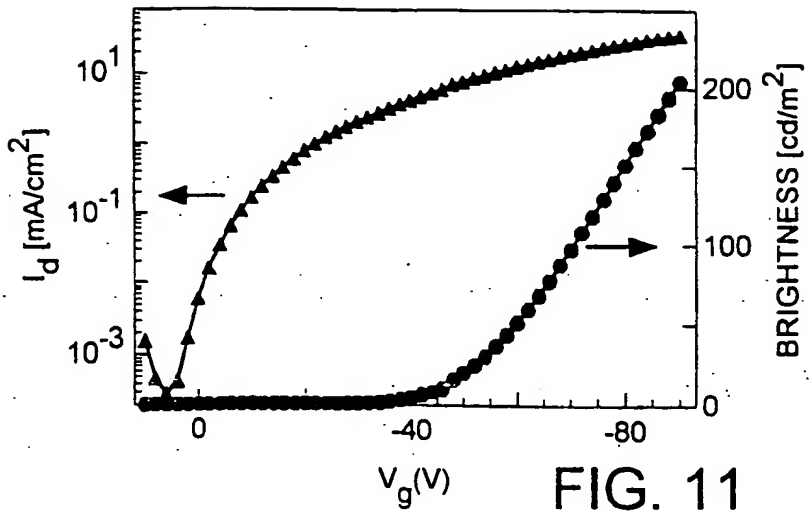
10^1
10^{-1}
10^{-3}
I_d [mA/cm^2]
200
100
0
BRIGHTNESS [cd/m^2]
0
-40
-80
V_g(V)

FIG. 11

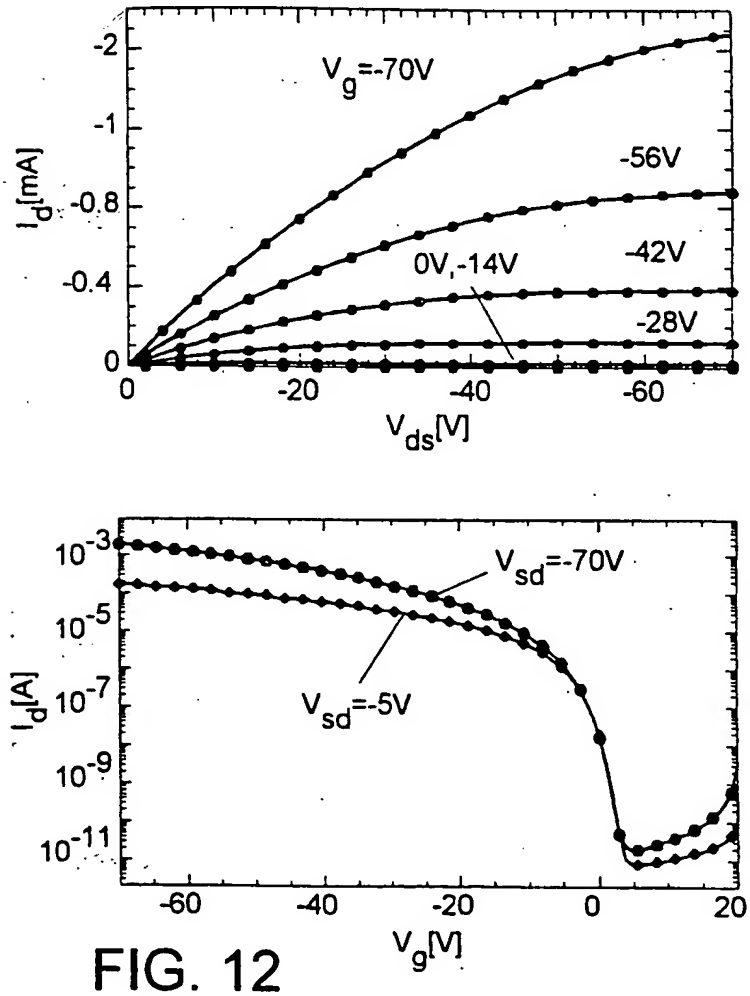
-2
-1
-0.8
-0.4
0
I_d[mA]
V_g=-70V
-56V
-42V
0V,-14V
-28V
0
-20
-40
-60
V_{ds}[V]
10^{-3}
10^{-5}
10^{-7}
10^{-9}
10^{-11}
I_d[A]
V_{sd}=-70V
V_{sd}=-5V
-60
-40
-20
0
20
V_g[V]

FIG. 12

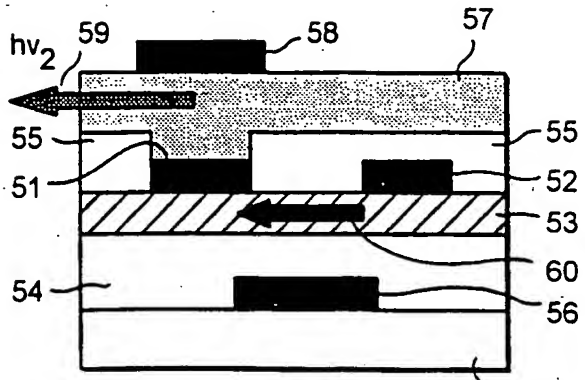

FIG. 13

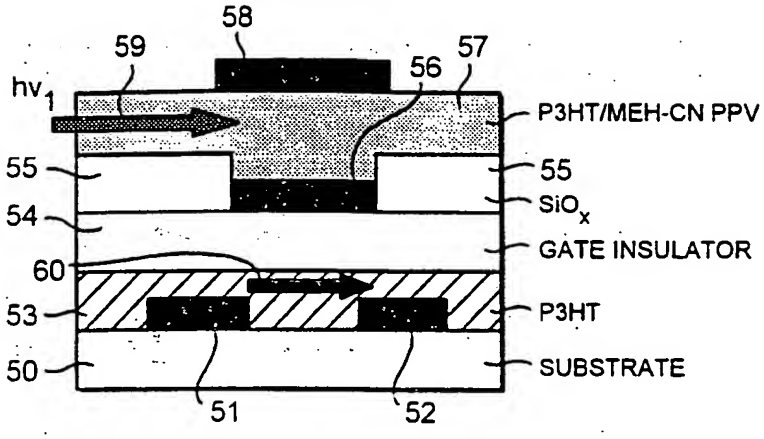

FIG. 14

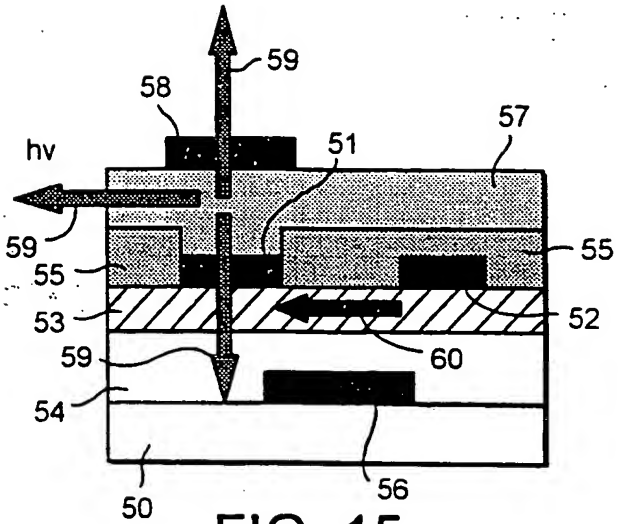

FIG. 15

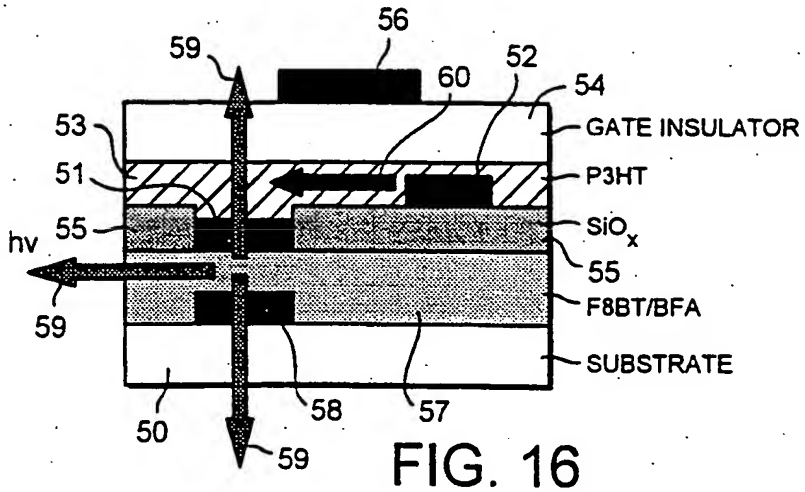

FIG. 16

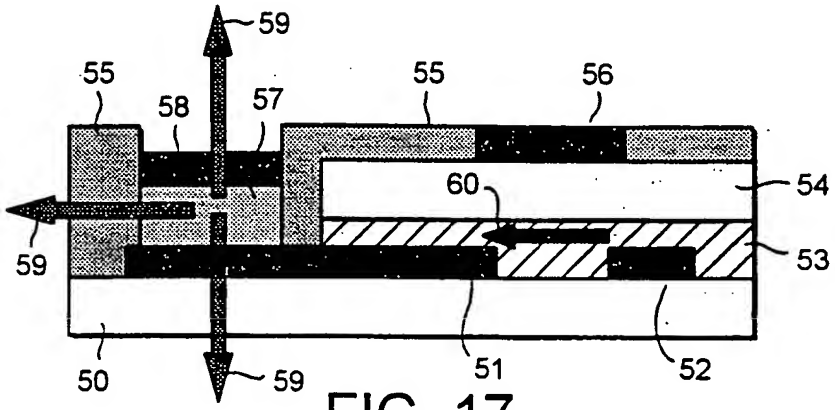

FIG. 17

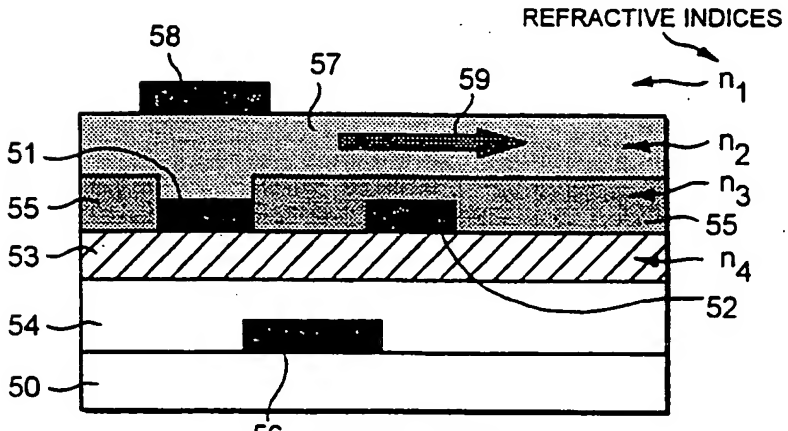

FIG. 18

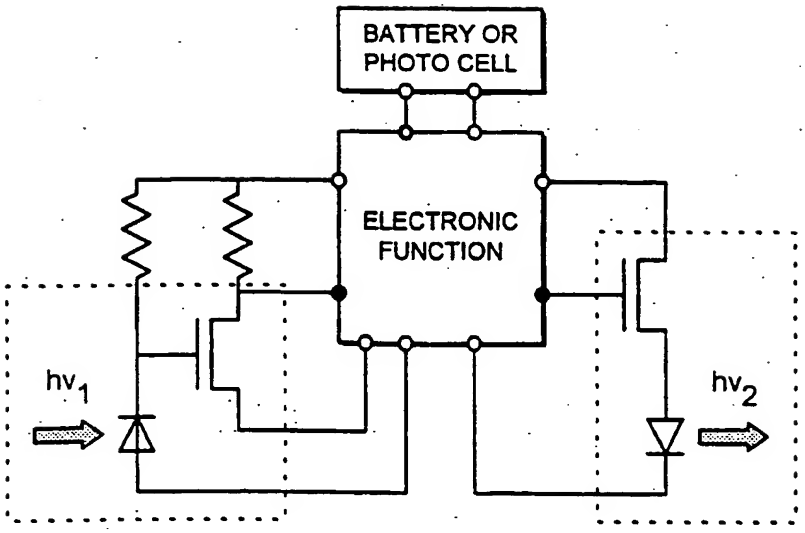
BATTERY OR
PHOTO CELL
ELECTRONIC
FUNCTION
hv1
hv2

FIG. 19

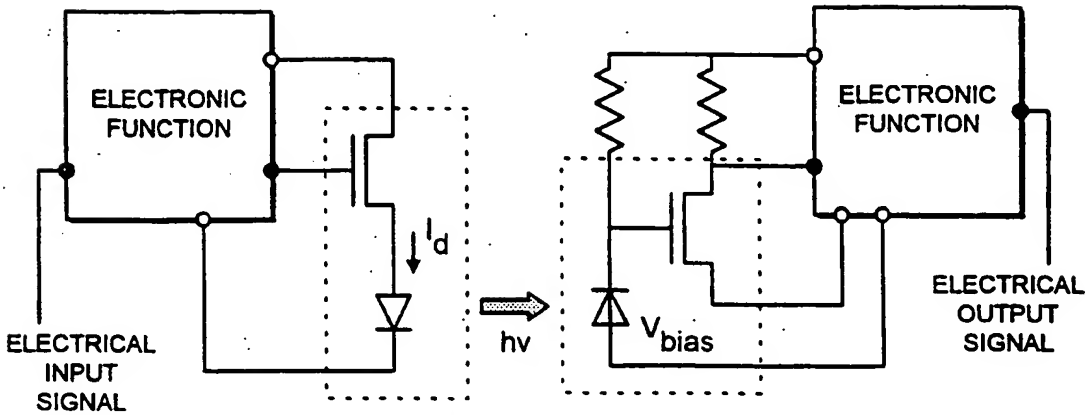
ELECTRONIC
FUNCTION
Id
ELECTRICAL
INPUT
SIGNAL
hv
Vbias
ELECTRONIC
FUNCTION
ELECTRICAL
OUTPUT
SIGNAL

FIG. 20

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 99/01176

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L27/00 H01L51/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 596 208 A (DODABALAPUR ANANTH ET AL) 21 January 1997 (1997-01-21) figures 2-4,10 ---	1,3,5,10
X	T. N. JACKSON, Y.-Y. LIN, D. J. GUNDLACH, H. KLAUK: "Organic Thin-Film Transistors for Organic Light-Emitting Flat-Panel Display Backplanes" IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, vol. 4, no. 1, January 1998 (1998-01), pages 100-104, XP002110213 the whole document ---	1,5-8, 10,21, 23,76-78
X	US 5 629 533 A (HARVEY III THOMAS B ET AL) 13 May 1997 (1997-05-13) the whole document ---	51,53
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 July 1999	12/08/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Königstein, C

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 99/01176

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DATABASE INSPEC 'Online! INSTITUTE OF ELECTRICAL ENGINEERS, STEVENAGE, GB MA E Y ET AL: "Organic light-emitting diode/thin film transistor integration for foldable displays" Database accession no. 6194905 XP002110246 abstract & CONFERENCE RECORD OF THE 1997 INTERNATIONAL DISPLAY RESEARCH CONFERENCE AND INTERNATIONAL WORKSHOPS ON LCD TECHNOLOGY AND EMISSIVE TECHNOLOGY, PROCEEDINGS OF 1997 INTERNATIONAL DISPLAY RESEARCH CONFERENCE AND WORKSHOPS, TORONTO, ONT., CANADA, 15-19 S, pages L78-L81, 1997, Santa Ana, CA, USA, Soc. Inf. Display, USA ---	1,6,7
X	BROWN A R ET AL: "LOGIC GATES MADE FROM POLYMER TRANSISTORS AND THEIR USE IN RING OSCILLATORS" SCIENCE, vol. 270, 10 November 1995 (1995-11-10), pages 972-974, XP000644682 ISSN: 0036-8075 the whole document ---	1
A	BROWN A R ET AL: "Field-effect transistors made from solution-processed organic semiconductors" SYNTHETIC METALS, 30 APRIL 1997, ELSEVIER, SWITZERLAND, vol. 88, no. 1, pages 37-55, XP002110216 ISSN: 0379-6779 the whole document ---	23-25, 31-34, 38,39
A	BAO Z ET AL: "SOLUBLE AND PROCESSABLE REGIOREGULAR POLY(3-HEXYLTHIOPHENE) FOR THIN FILM FIELD-EFFECT TRANSISTOR APPLICATIONS WITH HIGH MOBILITY" APPLIED PHYSICS LETTERS, vol. 69, no. 26, 23 December 1996 (1996-12-23), pages 4108-4110, XP002059693 ISSN: 0003-6951 ---	11-19
	-/--	

1

INTERNATIONAL SEARCH REPORT

Ir. ational Application No
PCT/GB 99/01176

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category '	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CARTER S A ET AL: "Polymeric anodes for improved polymer light-emitting diode performance" APPLIED PHYSICS LETTERS, 21 APRIL 1997, AIP, USA, vol. 70, no. 16, pages 2067-2069, XP002110222 ISSN: 0003-6951 the whole document	20
A	FR 2 360 177 A (UNIV EDINBURGH) 24 February 1978 (1978-02-24) the whole document	51,53,59
A	MASAHIRO HIRAMOTO ET AL: "UP-CONVERSION OF RED LIGHT TO GREEN BY A NEW TYPE OF LIGHT TRANSDUCER USING ORGANIC ELECTROLUMINESCENT DIODE COMBINED WITH PHOTORESPONSIVE AMORPHOUS SILICON CARBIDE" APPLIED PHYSICS LETTERS, vol. 58, no. 11, 18 March 1991 (1991-03-18), pages 1146-1148, XP000209773 ISSN: 0003-6951	
A	EP 0 575 187 A (MITSUBISHI CHEM IND ;MITSUBISHI ELECTRIC CORP (JP)) 22 December 1993 (1993-12-22) the whole document	

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int tional Application No
PCT/GB 99/01176

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5596208 A	21-01-1997	CA 2164357 A	10-06-1996
		EP 0716459 A	12-06-1996
		JP 8228034 A	03-09-1996
		SG 33622 A	18-10-1996
US 5629533 A	13-05-1997	NONE	
FR 2360177 A	24-02-1978	NONE	
EP 0575187 A	22-12-1993	JP 6005833 A	14-01-1994
		DE 69315895 D	05-02-1998
		DE 69315895 T	28-05-1998
		US 5350915 A	27-09-1994

CORRECTED VERSION*

PCT

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International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 27/00, 51/20

A1

(11) International Publication Number: WO 99/54936

(43) International Publication Date: 28 October 1999 (28.10.99)

(21) International Application Number: PCT/GB99/01176

(22) International Filing Date: 16 April 1999 (16.04.99)

(30) Priority Data:
9808061.7 16 April 1998 (16.04.98) GB

(71) Applicant *(for all designated States except US)*: CAMBRIDGE DISPLAY TECHNOLOGY LTD. [GB/GB]; 181a Huntingdon Road, Cambridge CB3 0DJ (GB).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: TESSLER, Nir [IL/GB]; 6 Teversham Way, Sawston, Cambridge CB2 4DF (GB). SIRRINGHAUS, Henning [DE/GB]; 33 Beaulands Close, Cambridge, CB4 1JA (GB). FRIEND, Richard, Henry [GB/GB]; 37 Barton Road, Cambridge CB3 9LG (GB).

(74) Agents: SLINGSBY, Philip, Roy et al.; Page White & Farrer, 54 Doughty Street, London WC1N 2LS (GB).

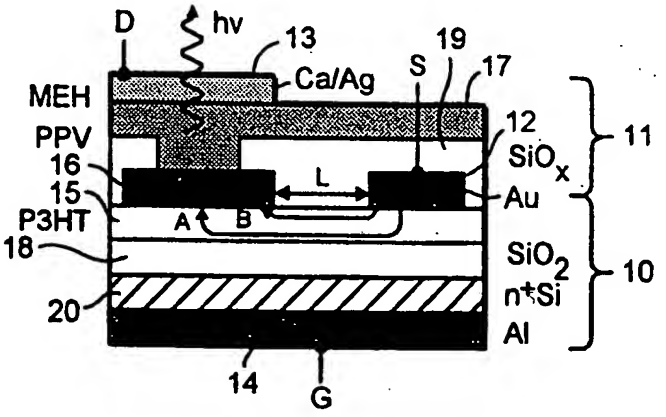
(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: POLYMER DEVICES

(57) Abstract

An integrated circuit device comprising: a current drive switching element having an input electrode, an output electrode, a switchable region comprising a semiconductive polymer material electrically coupled between the input electrode and the output electrode, and a control electrode electrically coupled to the switchable region so as to allow the application of a bias to the control electrode to vary the flow of current through the switchable region between the input electrode and the output electrode; and a second circuit element, integrated with the switching element, and electrically coupled with the input electrode of the switching element for receiving a drive current from the switching element.



*(Referred to in PCT Gazette No. 1/2000, Section II)

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L — A2

(11) International Publication Number: **WO 99/66540**

(43) International Publication Date: 23 December 1999 (23.12.99)

(21) International Application Number: PCT/NO99/00208

(22) International Filing Date: 18 June 1999 (18.06.99)

(30) Priority Data:

60/089,830	19 June 1998 (19.06.98)	US
19985729	8 December 1998 (08.12.98)	NO

(71) Applicant *(for all designated States except US)*: OPTICOM ASA [NO/NO]; P.O. Box 1872 Vika, N–0124 Oslo (NO).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: JACKSON, Thomas [US/US]; 1348 Deerfield Drive, State College, PA 16801 (US). BONSE, Mathias [DE/US]; Apartment 125, 201 Vairo Boulevard, State College, PA 16803 (US). THOMASSON, Daniel, B. [US/US]; 240 Los Alamos Road, Santa Rosa, CA 95409 (US). HAGEN, Klauk [DE/US]; Apartment B, 1670 West College Avenue, State College, PA 16801 (US). GUNDLACH, David, J. [US/US]; Apartment Fl, 445 Waupelani Drive, State College, PA 16801 (US).

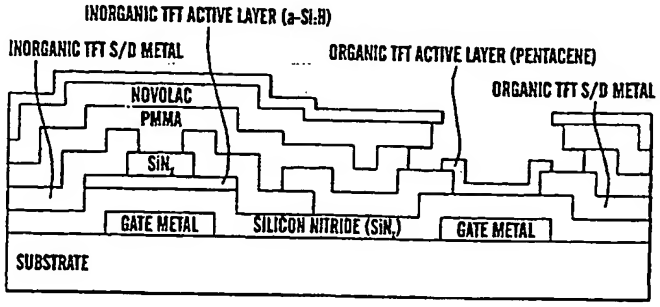
(74) Agent: LEISTAD, Geirr, I.; Opticom ASA, P.O. Box 1872 Vika, N–0124 Oslo (NO).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published

In English translation (filed in Norwegian).
Without international search report and to be republished upon receipt of that report.

(54) Title: INTEGRATED INORGANIC/ORGANIC COMPLEMENTARY THIN–FILM TRANSISTOR CIRCUIT



(57) Abstract

An integrated organic/inorganic complementary thin–film transistor circuit comprises a first and a second transistor which are operatively connected on a common substrate, wherein the first transistor is an inorganic thin–film transistor and the second an organic thin–film transistor. The inorganic thin–film transistor is an n–channel transistor and the organic thin–film transistor is a p–channel transistor or vice versa. Each of the transistors has a separate gate electrode and the organic active semiconductor material is in the case of a p–channel semiconductor in the organic thin–film transistor electrically isolated from the inorganic thin–film transistor. In a first method for fabricating a transistor circuit of this kind separate gate electrodes are deposited for each transistor on a common substrate, the material for the source and the drain electrode of the organic thin–film transistor are deposited on the same layer level in the thin–film structure of the organic thin–film transistor and in each case the organic active semiconductor material in an organic p–channel transistor is provided electrically isolated from the inorganic n–channel transistor, and the organic active semiconductor material in an organic n–channel transistor optionally electrically isolated from the inorganic p–channel transistor. In a more specific method for fabricating a complementary transistor circuit the inorganic active semiconductor is deposited in the form of hydrogenated amorphous silicon and an n^+ doped layer of a silicon material is deposited as respectively source and drain areas in the organic transistor. A layer of pentacene is deposited over an isolated layer which is patterned such that the pentacene which forms the active semiconductor in the organic thin–film transistor is isolated electrically from the inorganic thin–film transistor.

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Integrated inorganic/organic complementary thin-film transistor circuit.

The invention concerns an integrated inorganic/organic complementary thin-film transistor circuit, comprising a first and a second transistor which is operatively connected and provided on a common substrate, wherein the first transistor is an inorganic thin-film transistor and the second transistor an organic thin-film transistor, and wherein the complementary thin-film transistor circuit forms a multilayer structure.

The present invention also concerns methods for fabricating an integrated inorganic/organic complementary thin-film transistor circuit, comprising a first and a second transistor which are operatively connected and provided on a common substrate, wherein the first transistor is an inorganic thin-film transistor and the second transistor an organic thin-film transistor, and wherein the complementary thin-film transistor circuit forms a multilayer thin-film structure with successively deposited and patterned thin-film layers.

Integrated circuits of silicon realized as complementary metal-oxide semiconductors dominate the markets for a number of microelectronic applications such as microprocessors. But complementary circuits may also be of interest for more general application, e.g. in portable battery-operated electronic products, as they can provide very low static power dissipation for digital circuits. It has, however, turned out to be difficult to realize complementary integrated thin-film circuits with sufficient performance for commercial applications.

Hydrogenated thin-film transistors of silicon (a-Si:H TFT) have found a new application in thin-film components, particularly in liquid crystal displays with active matrix. However, complementary a-Si:H circuits are problematic, as the hole transport mobility typically is much lower than the electron transport mobility. Recently TFTs with organic active layers have been fabricated and with performance comparable to that which can be obtained with amorphous silicon devices (a-Si:H devices).

For instance there is in US patent no. 5 347 144 (Garnier & al.) disclosed a thin-film field-effect transistor with an MIS structure which includes a thin semiconductor layer between the source and drain electrode. The thin semiconductor layer contacts a surface of a thin-film made of isolating material which at its second surface contacts a conducting grid. The

semiconductor is made of at least one polyconjugated organic compound with a determined molecular weight. As organic semiconductor material Garnier & al. among others mention different various aromatic polycyclic hydrocarbons and among these polyacenes. The transistor of Garnier & al. is stated to be particularly suited as a switching or amplifying device.

Also simple organic complementary thin-film transistor circuits have been discussed in the literature, but have not shown the desired performance properties. Further attempts have been made building complementary circuits with combinations of inorganic and organic devices on separate substrates and with external connection.

In US patent no. 5 625 199 (Baumbach & al.) there is, however, disclosed a complementary circuit with an inorganic n-channel thin-film transistor and an organic p-channel thin-film transistor. The n-channel thin-film transistor employs hydrogenated amorphous silicon as active material and the p-channel of the organic thin-film transistor employs α-hexathienylene (α-6T) as active semiconductor material. The complementary thin-film transistor circuit according to Baumbach & al. can be used for implementing an integrated complementary inverter or other complementary circuits.

The integrated complementary inorganic/organic thin-film transistor according to Baumbach & al. is, however, encumbered with a number of disadvantages both from a processual point of view as well as with regard to general application in more comprehensive transistor circuits. Thus Baumbach & al. propose to provide respectively the source and drain electrodes on both sides of the organic semiconductor layer, something which firstly is not necessary and additionally comports a number of disadvantages in the fabrication. Further the source and drain contacts of the organic thin-film transistor must be formed in different steps and it will also be difficult to pattern contacts on the top of the organic semiconductor unless shadow masks are used.

Nor has the complementary thin-film transistor according to Baumbach an isolated organic semiconductor material in the organic thin film transistor. As it will be desirable to be able to turn the inorganic transistor on and to turn the organic transistor off or vice versa using potential with the same sign, this may be problematic. In the complementary thin-film transistor according to Baumbach & al, it is probable that an undesirable large leakage

will be problematic if the complementary thin-film transistor shall be used in complex circuits. An inverter realized according to Baumbach & al. switches as stated in the cited US patent at about 5V at a supply voltage of 7,2 V. Another disadvantage of the complementary thin-film transistor according to Baumbach & al. is that a common gate electrode is used both for the n-channel and the p-channel transistor. More complex transistor circuits built from complementary devices shall require that common electrodes are not used in these. Even in simple inverters a common gate electrode will give increased stray capacitance. Further it shall be remarked that the complementary thin-film transistor according to Baumbach & al. uses the inorganic transistor as n-channel transistor and the organic transistor as p-channel transistor, something which is understandable in light of the materials proposed. It is, however, evident from Baumbach & al. that the use of organic materials which may be used for forming active semiconductors of the n-type demands relatively complicated and costly fabricating processes and hence is not easy to realize for the time being.

A first object of the present invention is hence to overcome the disadvantages which are connected with prior art and particularly to provide an integrated complementary inorganic/organic thin-film transistor circuit which is suited for use in large transistor circuits. Another object is to provide complementary thin-film transistor circuits which allow a cheap fabrication and simultaneously have low static power consumption, such that they can be used in portable battery-operated equipment.

A further object of the present invention is to provide an uncomplicated and inexpensive method for fabricating integrated complementary inorganic/organic thin-film transistor circuits and this in as few process steps as possible, while a device with good electric properties is obtained and whereby it particularly shall be possible to realize the inorganic transistor as an n-channel transistor and the organic transistor as a p-channel transistor or vice versa.

The above-mentioned and other objects are achieved with an integrated inorganic/organic complementary thin-film transistor circuit which according to the invention is characterized in that the organic thin-film transistor is an n-channel transistor and that the organic thin-film transistor is a p-channel transistor, or vice versa, the organic active transistor material in each case

being respectively a p-channel organic semiconductor material or an n-channel organic semiconductor material, that separate gate electrodes are provided for each of the transistors, that the organic active semiconductor in an organic p-channel transistor in each case is provided electrically isolated from the inorganic n-channel transistor, and that the organic active semiconductor in an organic n-channel transistor optionally is provided electrically isolated from the inorganic p-channel transistor.

According to the invention the inorganic active semiconductor material is advantageously selected among hydrogenated amorphous silicon (a-Si:H), hydrogenated or unhydrogenated microcrystalline silicon (μc-Si:H;μc-Si), hydrogenated or unhydrogenated polycrystalline silicon (pc-Si:H;pc-Si), single crystal silicon. copper-doped polycrystalline germanium (pc-Ge:Cu), cadmium selenide (CdSe). cadmium telluride (CdTe), or composite inorganic semiconductors based on said materials. possibly in single crystal form.

Where the inorganic thin-film transistor is an n-channel transistor, the inorganic active semiconductor material is preferably amorphous silicon (a-Si:H), and where the inorganic transistor is a p-channel transistor, the inorganic active semiconductor material is preferably a p-channel silicon material, particularly p-channel hydrogenated amorphous silicon (a-Si:H).

In an advantageous embodiment the active semiconductor material in the inorganic thin-film transistor comprises at least one polyconjugated organic compound with a specific molecular weight. It is then advantageous that the polyconjugated organic compound or compounds are selected selected among conjugated oligomers. polycyclic aromatic hydrocarbons, particularly polyacenes. or polyenes.

Where the organic thin-film transistor is a p-channel transistor, it is advantageous that the organic active semiconductor material is pentacene, and where the organic thin-film transistor is an n-channel transistor, it is advantageous that the organic active semiconductor material is copper hexadecafluorophtalocyanide.

Finally, it is according to the invention particularly advantageous that the source electrode and the drain electrode of the organic thin-film transistor is provided in one and the same level in the thin-film structure of the organic thin-film transistor.

A first method for fabricating an integrated inorganic/organic complementary thin film transistor circuit is according to the invention characterized by forming the inorganic thin-film transistor as an n-channel transistor and the organic thin-film transistor as a p-channel transistor by depositing respectively an n-channel inorganic active semiconductor material and a p-channel organic active semiconductor material or correspondingly forming the organic thin-film transistor as an n-channel transistor and the inorganic thin-film transistor as a p-channel transistor by depositing respectively an n-channel organic active semiconductor material and a p-channel inorganic active semiconductor material, depositing separate gate electrodes for respectively the first and the second transistor on a common substrate, depositing material for the source electrode and the drain electrode of the organic thin-film transistor on the same level in the thin-film structure of the organic thin-film transistor and in each case providing the organic active semiconductor material in an organic p-channel transistor electrically isolated from the inorganic n-channel transistor and optionally providing the organic active semiconductive material in an organic n-channel transistor electrically isolated from the inorganic p-channel transistor.

A second method for fabricating an integrated inorganic/organic complementary thin-film transistor circuit is according to the invention characterized by comprising steps for depositing separate gate electrodes of a first metal for each of the two transistors on a common substrate, depositing separate inorganic isolators of silicon nitride (SiN_x) over each gate electrode, depositing an inorganic active semiconductor in the form of hydrogenated amorphous silicon (a-Si:H) above one of the gate electrodes which thus forms the gate electrode of the first transistor, depositing and patterning an n^+ doped layer of either hydrogenated amorphous silicon (n^+a-Si:H) or hydrogenated microcrystalline silicon ($n^+\mu$c-Si:H) or hydrogenated polycrystalline silicon (n^+pc-Si:H) as source and drain contacts for the first transistor, depositing and patterning the source and drain electrodes of the first transistor in form of a second metal over the source and drain contacts thereof, depositing and patterning the source and drain electrodes for the second transistor in the form of a third metal in the same layer level in the thin-film structure, forming an isolating double layer over the whole organic thin-film transistor and patterning this such that the source and drain electrodes and the gate isolator in the second transistor become exposed, whereafter a layer of pentacene is deposited above the isolating

double layer and the exposed portion of the second transistor, the pentacene layer in the exposed portion forming the active semiconductor material of the organic thin-film transistor and being provided electrically isolated against the additional pentacene layer broken by a re-entrant edge of the profile of the isolating double layer.

In an advantageous embodiment of the last-mentioned method according to the invention the steps for forming the inorganic thin-film transistor are realized in a tri-layer process which forms an inverted staggered three-layer structure.

In another advantageous embodiment of the last-mentioned method according to the invention the steps for forming the inorganic thin-film transistor are realized in a back-channel etch process.

In an advantageous embodiment of the last-mentioned method according to the invention the active semiconductor in the form of pentacene in the organic thin-film transistor is isolated by a re-entrant profile of a broken double layer of polymethylmetacrylate (PMMA) and Novolac photoresist.

In an advantageous embodiment of the last-mentioned method according to the invention gold is evaporated thermally for forming the source and drain electrodes of the organic thin-film transistor.

Finally, the pentacene layer which is deposited over the isolating double layer can optionally be removed.

The invention shall now be explained in more detail in connection with exemplary embodiments and with reference to the accompanying drawings wherein

fig. 1 shows a complementary thin-film transistor circuit according to prior art as exemplified by the above-mentioned US patent No. 5 675 199,

fig. 2a a first embodiment of the complementary thin-film transistor circuit according to the invention,

fig. 2b a second embodiment of a complementary thin-film transistor circuit according to the invention,

fig. 2c a variant of the embodiment in fig. 2b,

fig. 3a a third embodiment of the complementary thin-film transistor circuit according to the invention.

fig. 3b a fourth embodiment of the complementary thin-film transistor circuit according to the invention.

fig. 3c a fifth embodiment of the complementary thin-film transistor circuit according to the invention.

fig. 3d a variant of the embodiment in fig. fig. 3c,

figs. 4a-4r schematically the process steps in an embodiment of a method according to the present invention,

figs. 5a-5d a tri-layer etch process as used with a method according to the present invention.

figs. 6a-6c a back-channel etch process as used with a method according to the present invention.

fig. 7a schematically a section through an inverter realized with the complementary thin-film transistor circuit according to the present invention,

fig. 7b the circuit diagram of the inverter in fig. 7a.

fig. 7c a line drawing based on a microphotograph of the actual inverter in fig. 7a realized in thin film technology.

fig. 8a the voltage transfer curve for an inverter realized as in fig. 7a,

fig. 8b a diagram of the transient current for an inverter realized as in fig. 7a,

fig. 9a a line drawing based on a microphotograph of an actual NAND gate realized with complementary thin-film transistor circuits according to the present invention,

fig. 9b a circuit diagram of the NAND gate in fig. 9a,

fig. 9c the output voltage of the NAND gate in fig. 9a,

fig. 10 a line drawing based on a microphotograph of an actual five-stage ring oscillator realized with complementary thin-film transistor circuits according to the present invention,

fig. 11 the circuit diagram of the ring oscillator in fig. 10,

figs. 12a-12c respectively the gate delay, the power dissipation and the power dissipation product for the ring oscillator in fig. 10 as function of the supply voltage, and

figs. 13a-c respectively the gate delay, the power dissipation and the power dissipation product as function of the supply voltage for an eleven-stage ring oscillator realized with complementary thin-film transistor circuits according to the present invention.

First there shall now be given a discussion of prior art with the above-mentioned US patent No. 5 625 199 (Baumbach & al.) as starting point. Therein is disclosed a complementary circuit with inorganic n-channel thin-film transistor and an organic p-channel thin-film transistor, such as rendered in fig. 1. For both transistors a common gate electrode 2 of metal is provided on a substrate 1. Over the gate electrode is provided a dielectric 3 which forms the gate isolator and which typically is made of a non-conducting polymer. Over the gate isolator 3 then follows a layer 4 of undoped amorphous silicon which forms the active layer of the inorganic n-channel transistor. On the a-Si layer 4 is provided a patterned isolation layer 5 which serves to prevent short circuit between the source and drain areas of the n-channel transistor. Over the layers 3, 4 and 5 a further layer 6 of n^+ amorphous silicon has been deposited and provides electrical contact to the active amorphous silicon layer 4. The source/drain electrodes 7 are deposited patterned such that the source electrode and drain electrode of the n-channel transistor are not short-circuited. The metal layer 7 is besides patterned such that the n-channel and the p-channel transistors in the circuit are connected. Consequently the layer 7 extends towards the p-channel transistor and forms the source contact therein. Now follows a layer 8 of an isolating material, for instance silicon nitride, polyimide or another dielectric in order to isolate the source/drain electrodes 7 against the active organic semiconductor layer 9 which is formed of α-hexathienylene (α-6T) and which for instance may be deposited by vacuum sublimation. Finally, the prior art circuit comprises the drain electrode 10 of the p-channel transistor. The contact metal may be made of an evaporated or sputtered layer of Au or Ag and will be connected to the positive supply voltage. This prior art complementary transistor circuit is then in a final step coated with a

passivation layer 11. e.g. of silicon nitride or polyimide. to protect the circuit.

A section through a first embodiment of a complementary transistor circuit according to the present invention is shown in fig. 2a. Separate gate electrodes for respectively the inorganic and the organic transistor are deposited on a substrate and covered by a layer of silicon nitride which forms the gate isolator. The inorganic active semiconductor material is here shown in the form of hydrogenated amorphous silicon (a-Si:H) and provided such that it registers with the gate electrode of the inorganic transistor, but also extends beyond this where it forms n^+ doped areas for source and drain in the inorganic transistor. The contact material proper for the drain or source electrode is itself then deposited over the active semiconductor material and mutually isolated by a patterned isolation layer of silicon nitride. The material of the source electrode of the inorganic transistor may be of another metal than the metal in the gate electrode. Correspondingly the contact material for the source and drain electrodes of the organic transistor is deposited over the gate isolator such that the source and drain electrodes of the organic transistor in each case are located on the same level in the thin-film structure. Over both the inorganic and the organic transistors' source and drain contacts a double layer of respectively polymethylmetacrylate and Novolac photoresist is provided, but patterned such that the portion between the source and drain electrodes in the organic transistor is exposed, the isolating double layer in this area in section having a re-entrant profile. The organic active semiconductor material is now provided in the form of a layer over the isolating double layer where this has not been removed and in the exposed portion thereof, such that the semiconductor material contacts both the source and the drain electrodes of the organic transistor and simultaneously also registers with the gate electrode of organic transistor. The broken re-entrant profile and the isolating double layer provide a secure electrical isolation between the organic transistor and the inorganic transistor. Of course, the active organic semiconductor material optionally may be removed where it covers the isolating double layer. In fig. 2a it is, however, retained.

It is to be understood that the active inorganic semiconductor material is not restricted to a hydrogenated amorphous silicon, but may well consist of

hydrogenated microcrystalline or polycrystalline silicon. The source and drain material may also be deposited separately and be different from the channel area, e.g. n^+ doped microcrystalline hydrogenated silicon. Correspondingly the organic active semiconductor material in the organic transistor is not restricted to pentacene, but may generally be made of polyconjugated organic compounds with suitable properties and be formed by several such. As example of such polyconjugated organic compounds and as known in the art, it may be mentioned conjugated oligomers, the units of which includes or consists of phenylene groups which may be substituted, ortho-fused or ortho- and peri-fused aromatic polycyclic hydrocarbons with 4 to 20 fused rings, polyenes with the formula $H-C(T_1)=C(T_2)-H$ where T_1 and T_2 independently represent –H or a lower alkyl and r is an integer which may vary from 8 to 50, as well as conjugated oligomers whose repeating units contain at least a five-link heterocycle. Generally shall a polyconjugated compound used as active semiconductor material in the organic semiconductor transistor contain at least 8 conjugated bonds and have a molecular weight which is not greater than about 2000. For a more comprehensive discussion of these materials it shall besides be referred to the above-mentioned US patent no. 5 347 144 (Garnier & al.).

As an alternative to the embodiment in fig. 2a, the isolation of the active semiconductor material in the p-channel transistor may be achieved with a simplified version of the complementary thin-film transistor circuit. In fig. 2b this is shown by providing a photoresist layer over the complementary thin-film transistor circuit, whereafter the organic active semiconductor material is removed outside the organic thin-film transistor. The mask layer of the photoresist may be retained as shown in fig. 2b, but it may also be removed such this is shown in fig. 2c. In each case the active semiconductor material in the organic transistor becomes electrically isolated against the inorganic transistor. In that connection it shall be remarked that generally it has been regarded as a problem to remove active organic semiconductor material by etching, as such materials usually are damaged or destroyed when they are subjected to common photoresists and chemicals for treatment of the photoresist. However, it has turned out that a water-based etch process with water-based material provides very good results. In the patterning of e.g. organic optoelectronic material may e.g polyvinyl alcohol as solvent and gelatine as photoresist be an advantageous alternative. Besides are both

photolithography and printing other possible alternatives to etching – particularly printing may in the long run turn out to be both the simplest and cheapest.

Fig. 3a shows a section through an organic/inorganic thin-film transistor according to the present invention where an organic thin-film transistor with an n-channel organic semiconductor is employed. Fig. 3 shows the simplest embodiment possible, wherein separate gate electrodes are provided on the substrate, the gate isolator consists of the same material in both cases and the metal for the source/drain electrode similarly is the same for both transistors.

As an example of an organic n-channel material may be mentioned copper hexadecafluorophtalocyanine ($F_{16}CuPc$) (see Y.Y. Lin & al., "Organic complementary ringoscillators", Appl. Phys. Lett., Vol. 74 No. 18 (1999)). This organic semiconductor shows field-effect mobilities up to 10^{-2} cm/Vs and is not as sensitive to external conditions as other organic semiconductor materials of the n-type such as buckminsterfullerene (C_{60}).

Organic n-channel thin-film transistors based on copper-hexadecafluorophtalocyanine ($F_{16}CuPc$) or another organic semiconductor material of the n-type may be combined with one of several inorganic p-channel semiconductor materials in order to form the complementary thin-film transistor circuit.

As examples of suitable inorganic semiconductors of the p-type may be mentioned p-channel amorphous silicon which has field effect mobilities comparable with $F_{16}CuPc$, or copper-doped polycrystalline germanium (pc-Ge:Cu) which in the literature is shown used in combination with indium-doped cadmium selenide (Cd-Se:In) in a complementary polycrystalline thin-film technology (see J. Doutreloigne & al., "The electrical performance of a complementary CdSe:In/Ge:Cu thin film transistor technology for flat panel displays", Solid-State Electronics, Vol. 34 No. 2 (1991)). Polycrystalline germanium has displayed field-effect mobilities of about 5-15 cm^2/Vs, but requires a more complicated processing than amorphous silicon.

Fig. 3b shows an embodiment of the complementary thin-film transistor circuit according to the invention with an n-channel transistor. The embodiment in fig. 3b is analog to that in fig. 2a, but with the same metal used for the source and drain electrodes in both transistors. The isolating double layer may be realized as in fig. 2a, namely consisting of polymethylmetacrylate and Novolac photoresist such that the portion above the n-channel organic semiconductor is exposed, the isolating double layer also here being broken by a re-entrant profile. The active semiconductor in the n-channel organic transistor will then be isolated from the p-channel inorganic transistor, something which may be advantageous, but which is not a necessary condition for using an organic active n-channel semiconductor material.

The isolation of the organic active n-channel semiconductor material may also be achieved in corresponding manner as shown for the embodiment in fig. 2b, namely as shown in fig. 3c, where a photoresist is etched and masked such that the n-channel organic active semiconductor is isolated. The etch mask, i.e. the photoresist, may also here be removed from the organic n-channel transistor and it is then obtained the variant which is shown in fig 3d of the embodiment in fig. 3c.

There shall now with reference to figs. 4a-4r which schematically show the process scheme for integrated complementary a-Si:H organic transistor technology be given a description of specific features in the fabrication of the complementary thin-film transistor circuit according to the invention. The inorganic a-Si:H thin-film transistor is made in a process which provides an inverted staggered three-layer structure, something which shall be described more closely in the following . The layers of a-Si:H/SiN were deposited using of plasma-enhanced chemical vapour deposition. The subsequent process step comprises standard lithographic methods and wet etching techniques as well as sputtered deposition of source and drain metal for the inorganic thin-film transistor. The source and drain electrodes of the organic thin-film transistor were deposited by means of thermal evaporation. In order to isolate the active semiconductor material of the organic thin-film transistor, in this case pentacene, a re-entrant photoresist profile was used consisting of polymethylmetacrylate (PMMA) and Novolac photoresist which together forms an isolating double layer in the complementary transistor circuit. This is a necessary step, as thin-film transistors with pentacene as

p-channel active semiconductor material usually will have a positive threshold, i.e. a positive voltage must be used on the gate electrode to turn the transistor off. It is hence necessary to isolate an active p-channel semiconductor of pentacene in the organic transistor in order to prevent leakage in the pentacene layer, but as pentacene is sensitive to most forms of chemical processing, it is difficult to achieve isolation with the use of photolitography after the deposition of the organic semiconductive layer. With the method according to the invention the isolation is achieved during the deposition of the pentacene layer by breaking this over the re-entrant double-layer profile in the organic transistor. The maximum temperature which was used during the fabrication was 250°C.

Now the process steps for the fabrication of a transistor of this kind shall explicitly be discussed with a concrete short reference to figs. 4a-4r which, however, substantially will be self-explanatory to a person skilled in the art. In fig. 4a the gate electrode metal is deposited on the substrate by sputtering and then the separate gate electrodes are patterned with a first mask I as shown in fig. 4b. By means of plasma-enhanced chemical vapour deposition, a tri-layer structure is thereafter deposited, consisting of a gate isolator SiN_x over both gate electrodes, thereabove a layer of hydrogenated amorphous silicon and finally an isolation layer, once again formed of silicon nitride, such as shown in fig. 4c. In the subsequent step shown in fig. 4d a photoresist is now patterned with another mask II in order to actively define a thin-film transistor with hydrogenated amorphous silicon. In fig. 4e the uppermost silicon nitride layer is etched and in the subsequent process step in fig. 4f the layer of hydrogenated amorphous silicon is etched. In the process step shown in fig. 4g a photoresist is patterned for etching of i-stopper and the lowermost nitride layer by means of a third mask III. The etching itself of the i-stopper and the lowermost silicon nitride layer is shown in fig. 4h.

In order to realize the source and drain areas of the n-channel transistor as shown in fig. 4i n^+ a-Si:H is now deposited by means of plasma-enhanced chemical vapour deposition and in the subsequent process step in fig. 4j this takes place by means of a fourth mask IV for patterning a photoresist for lift-off of source/drain electrode metal. This is sputtered in the process step as shown in fig. 4k and is denoted with M2 which may be a metal different from the first metal used in the gate electrodes. In the process step shown in fig. 4l the source/drain metal M2 for the organic transistor was lifted off and

then follows in the process step shown in fig. 4m an etching of the n^+ layer of hydrogenated amorphous silicon which hence shall provide the source and drain areas of the inorganic transistor.

Now follows in the process step shown in fig. 4n a patterning of a photoresist for lift-off of the metallization of the organic thin-film transistor. This takes place by means of a fifth mask V. A metal layer of a third metal M3 is now deposited over the whole transistor circuit, as shown in fig. 4o, and then follows the lift-off of this metal layer M3, such that the organic thin-film transistor appears with source and drain electrodes of the metal M3 provided in the same level in the thin-film structure. In order to isolate the organic thin-film transistor electrically against the inorganic thin-film transistor is now by means of photo-lithography deposited a double layer consisting of polymethylmetacrylate PMMA and for instance Novolac photoresist. The isolating double layer is patterned such that the source and drain electrodes of the metal M3 for the organic thin-film transistor are exposed between re-entrant broken profiles of the isolating double layer, such this is shown in fig. 4q. Finally is now the organic active semiconductor material deposited in the form of pentacene over the whole circuit and provides in the exposed portion the active p-channel semiconductor material of the organic transistor. It shall be understood that the pentacene layer where it covers the isolating double layer besides may be removed therefrom in a concluding not shown process step. Further may, of course, electrically isolating passivation and planarization layers be deposited over the whole complementary thin-film circuit, such this is known in the art, but not here specifically shown. The complementary organic thin-film transistor circuit according to the invention now appears substantially as shown in fig. 4r and corresponding to the embodiment shown in fig. 2a.

The tri-layer etch process as used with the present invention and as rendered in the process steps as shown in figs. 4c-h shall now be discussed in somewhat greater detail with reference to figs. 5a-5d. In the tri-layer etch process as shown in fig. 5a, a triple layer of silicon nitride, undoped hydrogenated amorphous silicon and a further layer of silicon nitride are deposited on the patterned gate electrode. The uppermost silicon nitride layer is patterned as shown in fig. 5b and an n^+ doped layer of amorphous hydrogenated silicon is deposited all over as shown in fig. 5c. The metal of the source and drain electrodes is patterned and the doped amorphous silicon

material over the uppermost silicon nitride layer etched away, as shown in fig. 5d. As the uppermost silicon nitride layer protects the channel area in the inorganic thin-film transistor, this etch step is not critical. However, the tri-layer process requires two deposition steps of amorphous silicon and as the source and drain electrodes must be patterned on the top of the uppermost silicon nitride layer which is patterned with the channel length, this requires a more aggressive photolithography for a given channel length.

The back-channel etch process is shown in fig. 6a-6c. An isolation layer of silicon nitride is deposited over the gate electrode and the substrate, and followed by undoped hydrogenated silicon and n^+ doped silicon as well as a further layer of n^+ doped hydrogenated amorphous silicon. This is shown in fig. 6a. The source and drain electrodes are patterned and the doped hydrogenated amorphous silicon in the channel area is etched away, such this is shown in fig. 6b and fig. 6c respectively. The back-channel etch process is very simple. but the etching of the n^+ doped hydrogenated amorphous silicon in the channel area is a critical step. Typically back-channel etching results in inorganic thin-film transistors with poorer quality than that may be obtained by using a three-layer etch process.

Fig. 7a shows a schematic section through an inverter formed with the integrated complementary thin-film transistor circuit according to the invention. Functionally the inverter in fig. 7a corresponds substantially to the complementary transistor circuit according to prior art as rendered in fig. 1, but is based on the embodiment according to the present invention such this for instance is shown in fig. 2a. As therein the organic transistor of the inverter is based on a p-channel semiconductor material, viz. pentacene, and hydrogenated amorphous silicon in doped and undoped form is used as the semiconductor material in the inorganic transistor. As the input signal to the inverter shall be conveyed to the gate electrodes, there is for this purpose provided a gate electrode contact as shown to left in fig. 7a. This gate electrode contact may then be deposited in the same process step as shown in fig. 4a-4b with the use of mask I. As in fig. 2a the isolating double layer of polymethylmetacrylate on Novolac photoresist will isolate both the organic transistor as well as the inverter gate contact against the inorganic transistor. Besides may also here the pentacene layer which is provided over the isolating double layer as well as over the gate electrode contact of the inverter. be removed. The well-known schematic circuit diagram of the

inverter shown in fig. 7b and an inverter realized with use of a complementary transistor circuit and a method according to the invention is shown by the line drawing in fig. 7c. The organic thin-film transistor is here located at left and the inorganic thin-film transistor in the complementary thin-film transistor circuit at right in fig. 7c.

Fig. 8a shows the voltage transfer curves for different supply voltages for an inverter with a β ratio of 1. The β ratio is here defined by

$$\beta = \frac{(W/L)_{a\text{-}Si:H}}{W/L_{pentacene}}$$

In this regard it shall be remarked that in CMOS circuits both transistors may be operated both as driver and load. Due to a topological similarity β is sometimes defined as the width/length relationship W/L for the n-channel device divided by the length/width relationship for the p-channel device. – The inverter shows sharp transitions with a gain which exceeds 22 for a supply voltage of 20 V. The on voltage of the inverter is equal to the supply voltage and the off voltage is 0 V. This shows the complete maintenance of the voltage levels of the complementary thin-film transistor circuit according to the invention. The transition current for the inverter reaches a top near the logic transition voltage and is otherwise very low, such this is evident from fig. 8b. This shows that the complementary thin-film transistor circuit according to the present invention has a true complementary behaviour.

With the complementary thin-film transistor circuit according to the present invention it is, of course, possible to realize logic gates as otherwise well-known in the CMOS-technology. An example of a complementary NAND-gate realized by means of a complementary transistor circuit according to the present invention is shown in the line drawing in fig. 9a and the corresponding schematic circuit diagram in fig. 9b. By connecting the output of the NAND gate to the inverter shown in fig. 7c a complementary AND gate is of course obtained, the output of which then becoming the inverted of the output signal from the NAND gate. The voltage transfer curve for different input voltages for the NAND gate is shown in fig. 9c and has the same properties as the voltage transfer curves for the simple inverter such these are shown in fig. 8a. A person skilled in the art will, of course, realize that generally may all logic gates as known in the CMOS technology and the corresponding Boolean functions be realized with the use of a NAND gate as

shown in fig. 9a and inverters as shown in fig. 7c. The integrated complementary thin-film transistor circuit according to the invention is generally used for realizing logic gates in complementary thin-film technology.

By means of the integrated complementary thin-film circuits ring oscillators were made with respectively 5 and 11 inverter stages and with different β ratios. These ring oscillators show a single gate delay as low as 5 μs, a gate power dissipation less than 0.2 μW per stage and a power delay product as low as 15 pJ. The gate delay decreases fast with the increasing supply voltage, such that high operating frequencies may be obtained with the relatively low supply voltage.

A line drawing of a five-stage ring oscillator is shown in fig. 10 and with the circuit diagram rendered in fig. 11. In addition to the five inverter stages an additional sixth inverter is used for isolating the circuit from the capacity load of an oscilloscope used for measuring the characteristics of the ring oscillator. From the measured oscillation frequency the delay of a single inverter stage can be derived. Fig. 12a shows the single gate delay for the shown five-stage ring oscillator, fig. 12b power dissipation and fig. 12c the power delay product for the same, all figures showing these characteristics for a β ratio of 1/2.

A ring oscillator with eleven inverter steps is realized in corresponding manner with the use of the integrated complementary thin-film circuit according to the present invention, but not shown herein. Fig.13a, 13b and 13c, however, show the corresponding characteristics for this eleven-stage ring oscillator as shown in fig. 12a-12c, but with a β ratio of 1/3.

The methods according to the present invention are simple and hence make it possible to fabricate integrated complementary thin-film transistor circuits according to the invention at low costs. Complementary transistor circuits have an inherent low static power consumption, something which is of importance for applications based on battery power. This makes the complementary thin-film transistor circuit according to the invention applicable in control circuits for liquid crystal displays in portable PCs, so-called "lap-tops" or for low-level implementation such as programmable tags. The circuits according to the invention have high switching amplification and very good maintenance of the logic level in addition to low

static power consumption. The gate delay in the transistor circuits fabricated according to the invention measured by means of ring oscillators is as mentioned as low as 5μs, the fastest speed up to now obtained with circuits which use organic transistors.

The hybrid integrated complementary thin-film technology, wherein the organic thin-film transistor may be an n-channel transistor and the organic transistor a p-channel transistor or vice versa, is of course, not restricted to use of the active semiconductor materials as mentioned in the exemplary embodiments. The on-going development of suitable organic as well as inorganic semiconductor materials makes it probable that in the future both n- as well as p-channel active organic semiconductor materials and correspondingly n- as well as p-channel inorganic active semiconductor materials with further improved properties may be employed. Composite inorganic semiconductor compounds may be of interest and the same applies to single crystal silicon, while on the other hand gallium arsenide for the time being appears less probable, but shall in no way be excluded in future hybrid complementary thin-film transistor circuits of the kind disclosed herein.

CLAIMS

1. An integrated inorganic/organic complementary thin-film transistor circuit comprising a first and a second transistor which are operatively connected and provided on a common substrate, wherein the first transistor is an inorganic thin-film transistor and the second transistor an organic thin-film transistor, and wherein the complementary thin-film transistor circuit forms a multilayer thin-film structure, characterized in that the inorganic thin-film transistor is an n-channel transistor and that the organic thin-film transistor is a p-channel transistor, or vice versa, the organic active transistor material in each case being respectively a p-channel organic semiconductor material or an n-channel organic semiconductor material,
that separate gate electrodes are provided for each of the transistors,
that the organic active semiconductor in an organic p-channel transistor in each case is provided electrically isolated from the inorganic n-channel transistor, and
that the organic active semiconductor in an organic n-channel transistor optionally is provided electrically isolated from the inorganic p-channel transistor.

2. A complementary thin-film transistor circuit according to claim 1, characterized in that the inorganic active semiconductor material is selected among hydrogenated amorphous silicon (a-Si:H), hydrogenated or unhydrogenated microcrystalline silicon (μc-Si:H;μc-Si), hydrogenated or unhydrogenated polycrystalline silicon (pc-Si:H;pc-Si), single crystal silicon, copper-doped polycrystalline germanium (pc-Ge:Cu), cadmium selenide (CdSe), cadmium telluride (CdTe), or composite inorganic semiconductors based on said materials, possibly in single crystal form.

3. A complementary thin-film transistor circuit according to claim 2 wherein the inorganic transistor is an n-channel transistor, characterized in that the inorganic active semiconductor material is hydrogenated amorphous silicon (a-Si:H).

4. A complementary thin-film transistor circuit according to claim 2, wherein the inorganic transistor is a p-channel transistor, characterized in that the inorganic active semiconductor material is a

p-channel silicon material, particularly p-channel hydrogenated amorphous silicon (a-Si:H).

5. A complementary thin-film transistor circuit according to claim 1, characterized in that the active semiconductor material in the organic thin-film transistor comprises at least one polyconjugated organic compound with a specific molecular weight.

6. A complementary thin-film transistor circuit according to claim 5, characterized in that the polyconjugated organic compound or compounds are selected among conjugated oligomers, polycyclic aromatic hydrocarbons, particularly polyacenes, or polyenes.

7. A complementary thin-film transistor circuit according to claim 6, wherein the organic thin-film transistor is a p-channel transistor, characterized in that the organic semiconductor material is pentacene.

8. A complementary thin-film transistor circuit according to claim 1, wherein the organic thin-film transistor is an n-channel transistor, characterized in that the organic active semiconductor material is copper hexadecafluorophtalocyanide ($F_{16}CuPc$).

9. A complementary thin-film transistor circuit according to claim 1, characterized in that the source electrode and the drain electrode of the organic thin-film transistor are provided in one and the same level in the thin-film structure of the organic thin-film transistor.

10. A method for fabricating an integrated inorganic/organic complementary thin-film transistor circuit comprising a first and a second transistor which are operatively connected and provided on a common substrate, wherein the first transistor is an inorganic thin-film transistor and the second transistor a organic thin-film transistor, and wherein the complementary thin-film transistor circuit forms a multilayer thin-film structure with successively deposited and patterned thin-film layers, characterized by forming the inorganic thin-film transistor as an n-channel transistor and the organic thin-film transistor as a p-channel transistor by depositing respectively an n-channel inorganic active semiconductor material and a p-channel organic active semiconductor material or correspondingly forming the organic thin-film transistor as an n-channel transistor and the inorganic thin-film transistor as a p-channel transistor by depositing

respectively an n-channel organic active semiconductor material and a p-channel inorganic active semiconductor material, depositing separate gate electrodes for respectively the first and the second transistor on a common substrate, depositing material for the source electrode and the drain electrode of the organic thin-film transistor on the same level in the thin-film structure of the organic thin-film transistor and in each case providing the organic active semiconductor material in an organic p-channel transistor electrically isolated from the inorganic n-channel transistor and optionally providing the organic active semiconductive material in an organic n-channel transistor electrically isolated from the inorganic p-channel transistor.

11. A method for fabricating an inorganic/organic complementary thin-film transistor circuit comprising a first and a second transistor which are operatively connected and provided on a common substrate, wherein the first transistor is an inorganic thin-film transistor and the second transistor an organic thin-film transistor, wherein the complementary thin-film transistor circuit forms a multilayer thin-film structure with successively deposited and patterned thin-film layers, and wherein the method is characterized by comprising steps for depositing separate gate electrodes of a first metal for each of the two transistors on a common substrate,
depositing separate inorganic isolators of silicon nitride (SiN_x) over each gate electrode,
depositing an inorganic active semiconductor in the form of hydrogenated amorphous silicon (a-Si:H) above one of the gate electrodes which thus forms the gate electrode of the first transistor, depositing and patterning an n^+ doped layer of either hydrogenated amorphous silicon (n^+a-Si:H) or hydrogenated microcrystalline silicon ($n^+\mu$c-Si:H) or hydrogenated polycrystalline silicon (n^+pc-Si:H) as source and drain contacts for the first transistor, depositing and patterning the source and drain electrodes of the first transistor in form of a second metal over the source and drain contacts thereof, depositing and patterning the source and drain electrodes for the second transistor in the form of a third metal in the same layer level in the thin-film structure, forming an isolating double layer over the whole organic thin-film transistor and patterning this such that the source and drain electrodes and the gate isolator in the second transistor become exposed, whereafter a layer of pentacene is deposited above the isolating double layer and the exposed portion of the second transistor, the pentacene layer in the exposed portion forming the active semiconductor material of the organic

thin-film transistor and being provided electrically isolated against the additional pentacene layer broken by a re-entrant edge of the profile of the isolating double layer.

12. A method according to claim 11, characterized by realizing the steps for forming the inorganic thin-film transistor in a tri-layer process which forms an inverted staggered tri-layer structure.

13. A method according to claim 11, characterized by realizing the steps forming the inorganic thin-film transistor in a back-channel etch process.

14. A method according to claim 11, characterized by isolating the active semiconductor in the form of pentacene in the organic thin-film transistor by a re-entrant profile of a broken double layer of polymethylmetacrylate (PMMA) and Novolac photoresist.

15. A method according to claim 11, characterized by evaporating gold thermally for forming the source and drain electrodes of the organic thin-film transistor.

16. A method according to claim 11. characterized by optionally removing the pentacene layer which has been deposited over the isolating double layer.

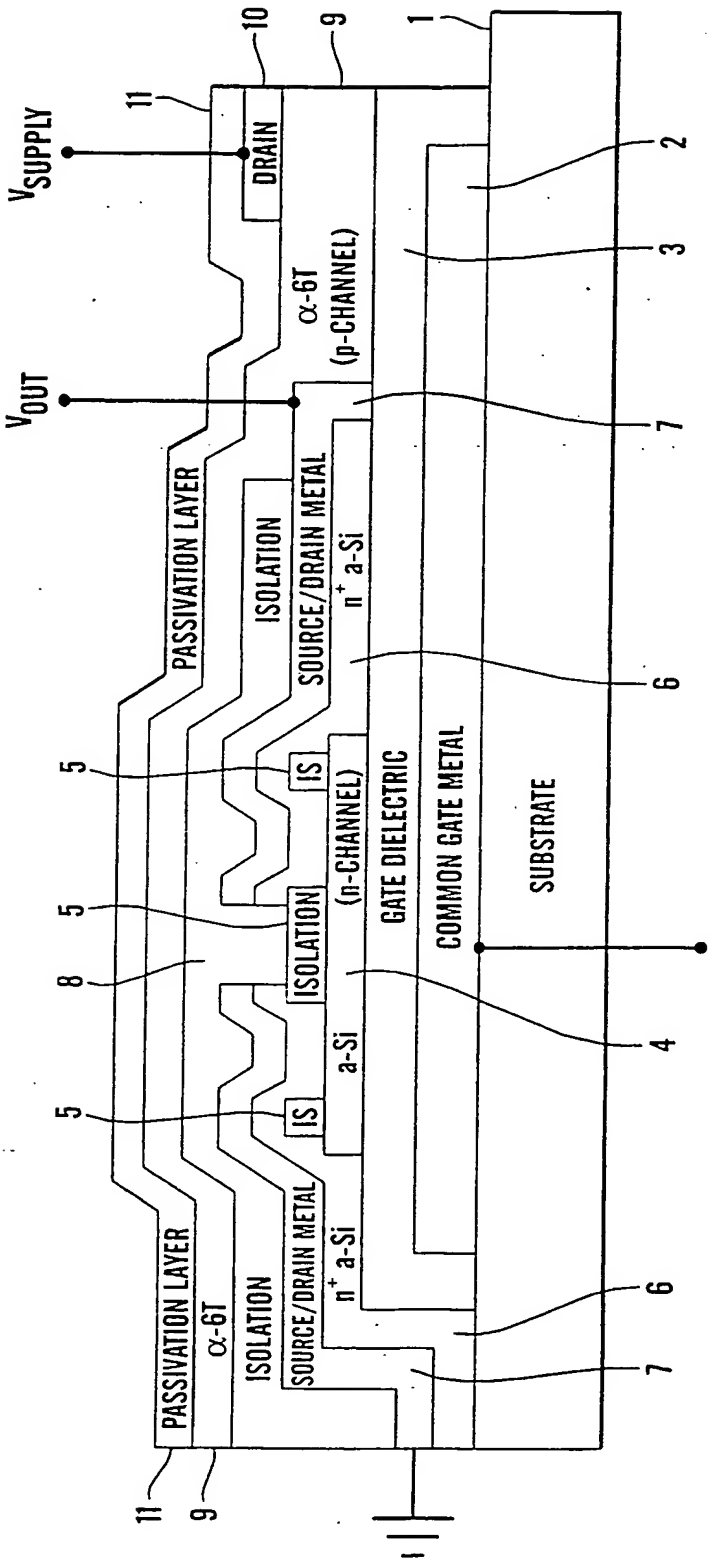

Fig. 1 (PRIOR ART)

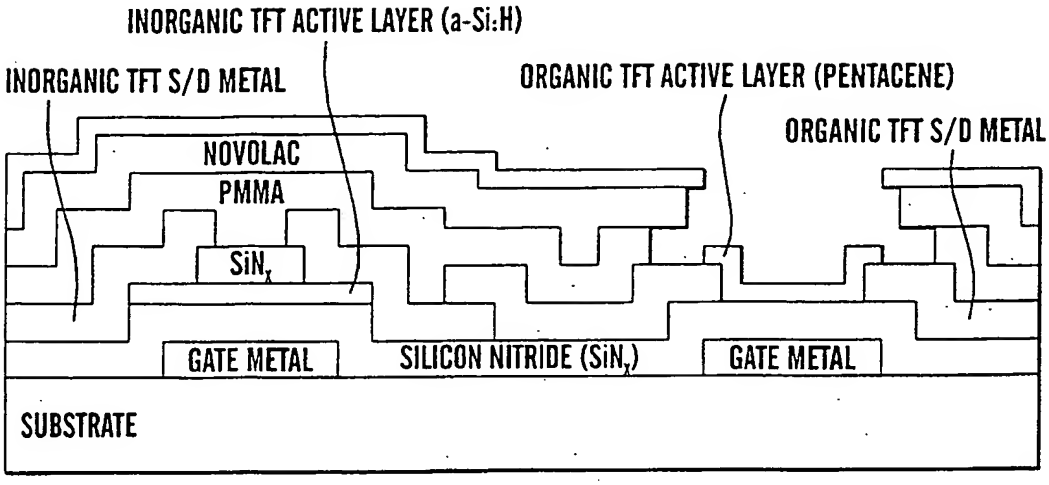

Fig.2a

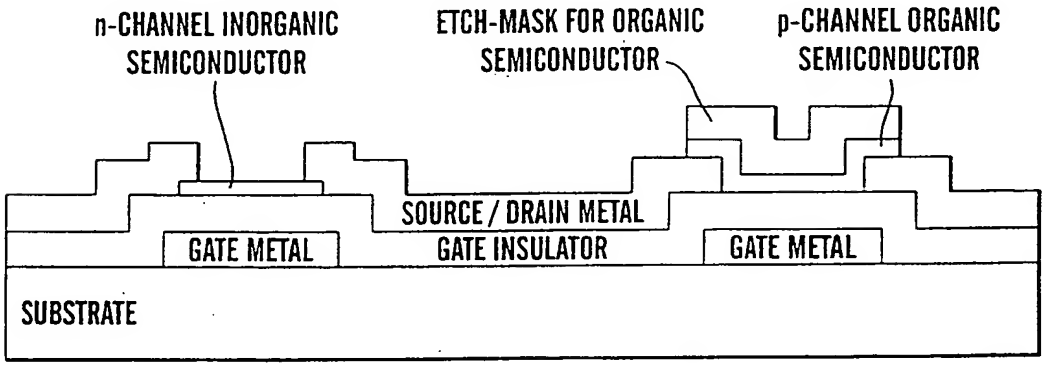

Fig.2b

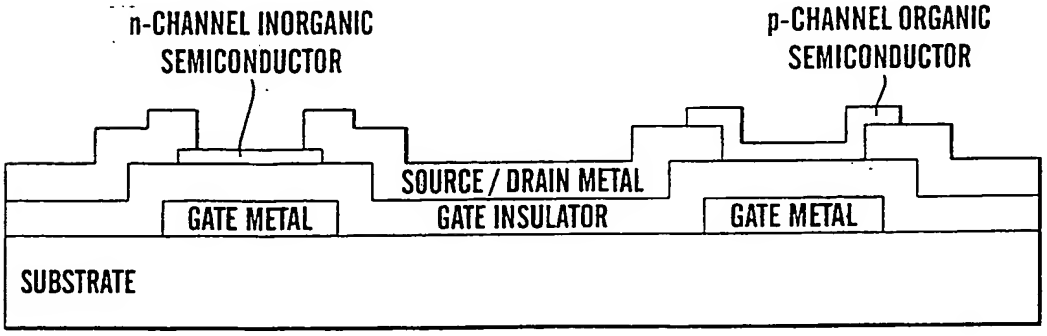

Fig.2c

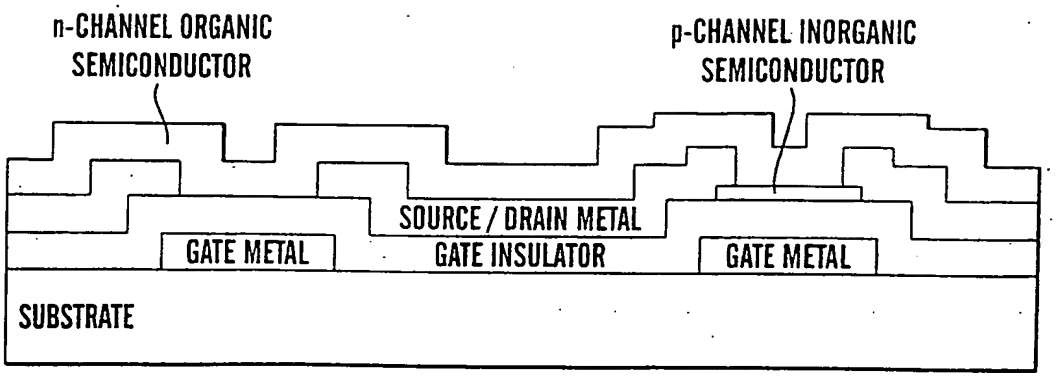
n-CHANNEL ORGANIC SEMICONDUCTOR
p-CHANNEL INORGANIC SEMICONDUCTOR
SOURCE / DRAIN METAL
GATE METAL
GATE INSULATOR
GATE METAL
SUBSTRATE

Fig.3a

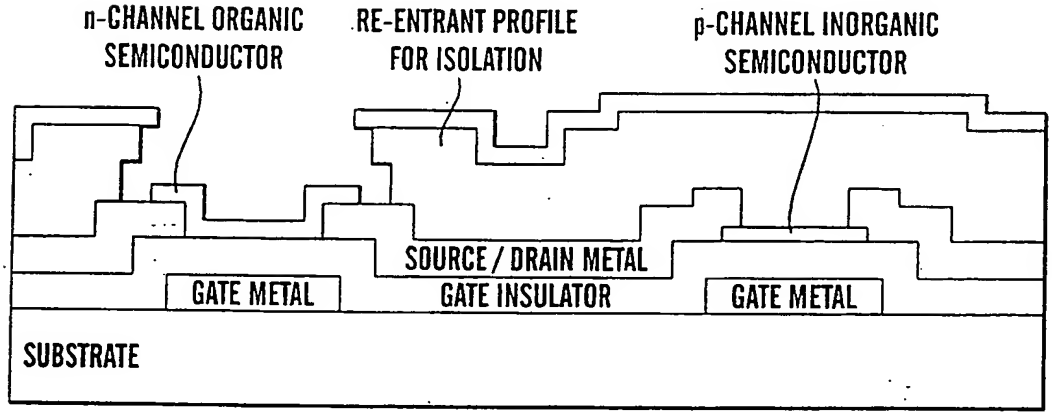
n-CHANNEL ORGANIC SEMICONDUCTOR
RE-ENTRANT PROFILE FOR ISOLATION
p-CHANNEL INORGANIC SEMICONDUCTOR
SOURCE / DRAIN METAL
GATE METAL
GATE INSULATOR
GATE METAL
SUBSTRATE

Fig.3b

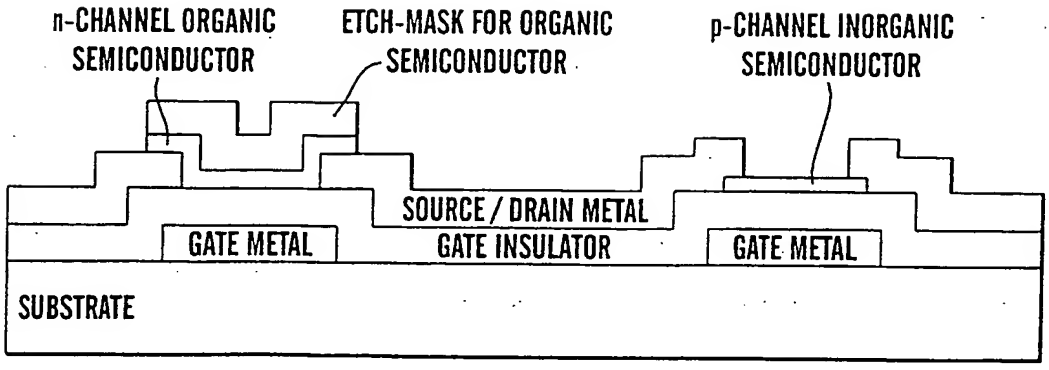
n-CHANNEL ORGANIC SEMICONDUCTOR
ETCH-MASK FOR ORGANIC SEMICONDUCTOR
p-CHANNEL INORGANIC SEMICONDUCTOR
SOURCE / DRAIN METAL
GATE METAL
GATE INSULATOR
GATE METAL
SUBSTRATE

Fig.3c

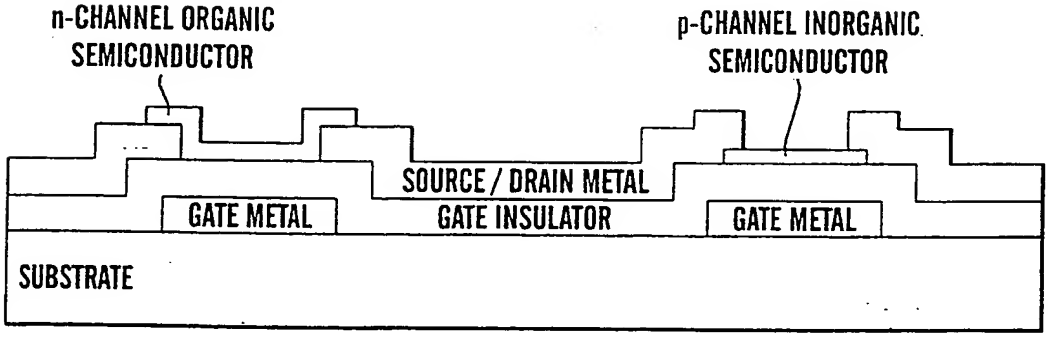
n-CHANNEL ORGANIC SEMICONDUCTOR
p-CHANNEL INORGANIC SEMICONDUCTOR
SOURCE / DRAIN METAL
GATE METAL
GATE INSULATOR
GATE METAL
SUBSTRATE

Fig.3d

SPUTTER OF GATE METAL:

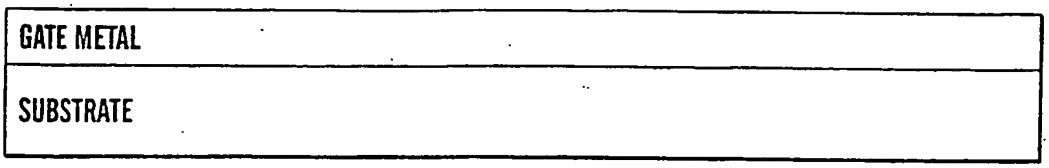

Fig.4a

DEFINITION OF GATE METAL PATTERN (MASK I):

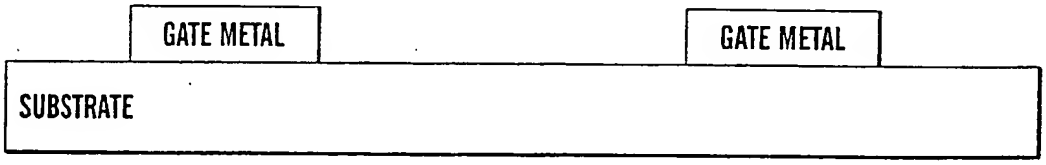

Fig.4b

PECVD OF TRI-LAYER:

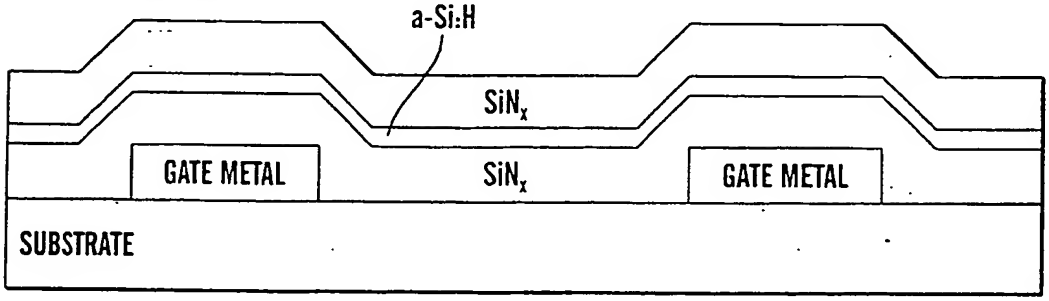

Fig.4c

PATTERING OF PHOTORESIST FOR ACTIVE DEFINITION OF a-Si:H TFTs (MASK II):

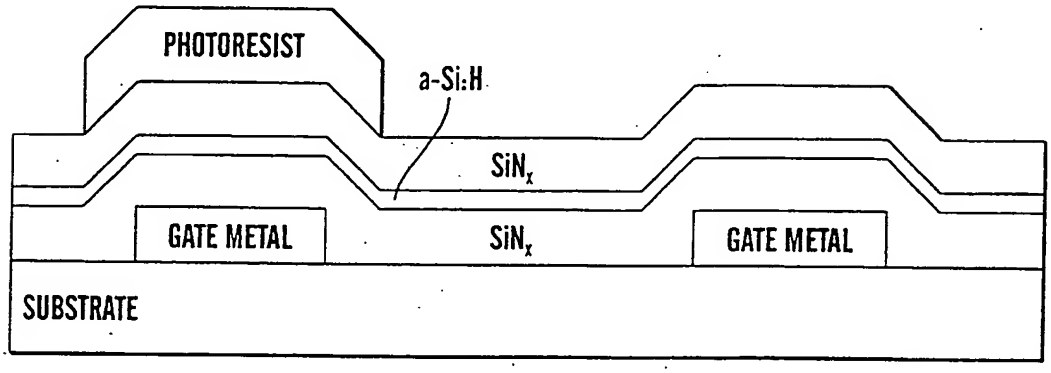

Fig.4d

ETCHING OF TOP NITRIDE LAYER:

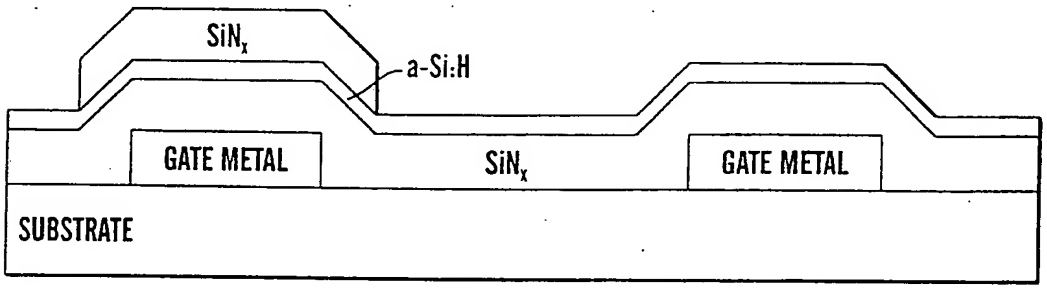

Fig.4e

ETCHING OF a-Si:H LAYER:

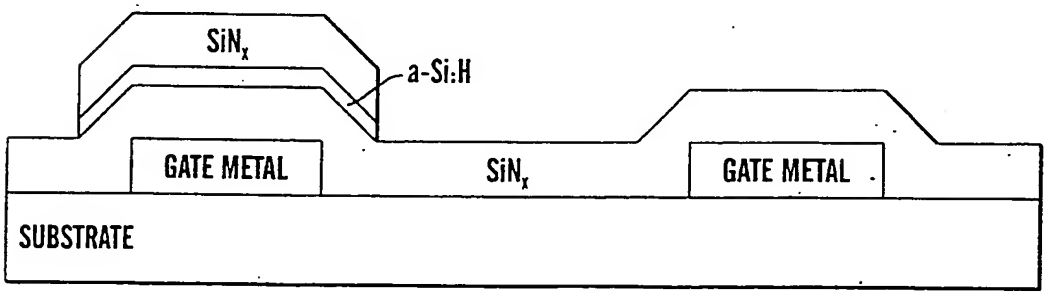

Fig.4f

PATTERNING OF PR FOR ETCH OF I-STOPPER AND BOTTOM NITRIDE LAYER (MASK III):

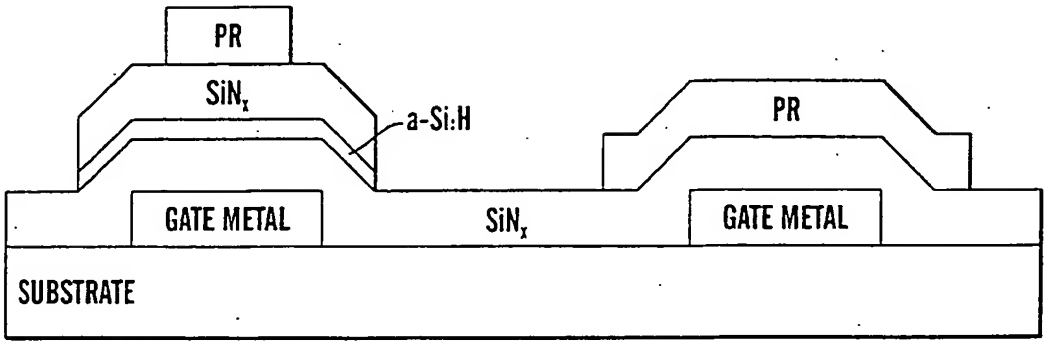

Fig.4g

ETCHING OF I-STOPPER AND BOTTOM NITRIDE LAYER:

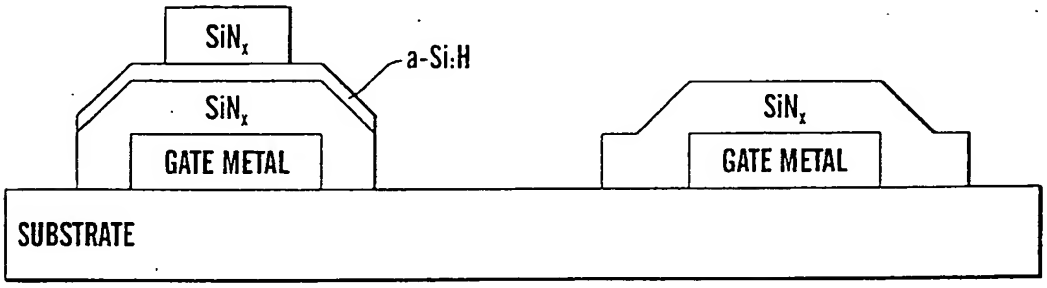

Fig.4h

PECVD OF n^+ a-Si:H:

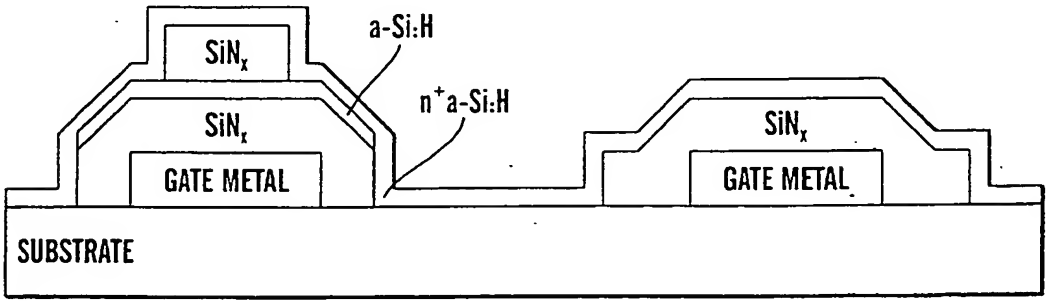

Fig.4i

PATTERNING OF PR FOR LIFTOFF (MASK IV):

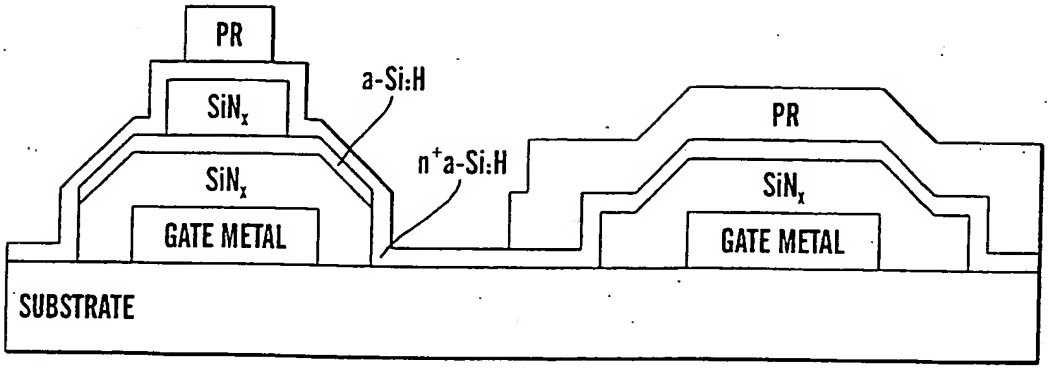

Fig.4j

SPUTTERING OF SOURCE / DRAIN METAL OF a-Si:H TFTs:

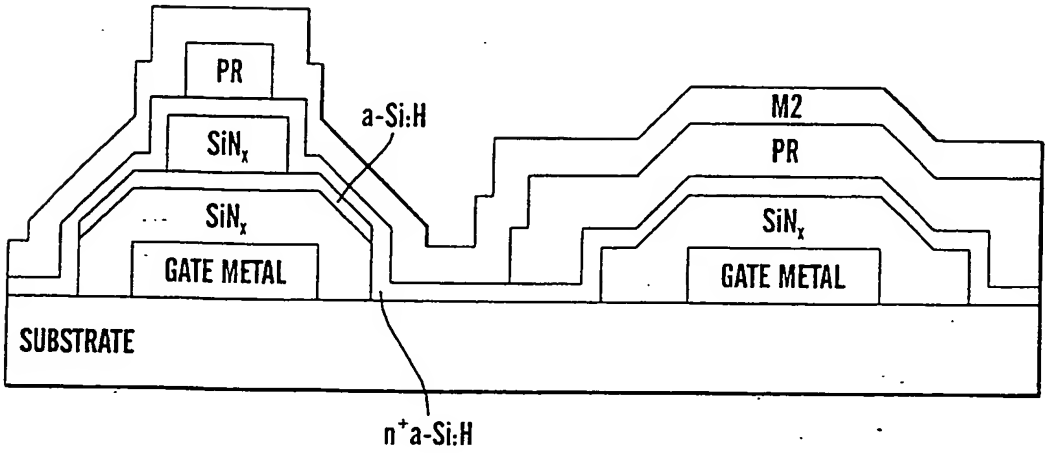

Fig.4k

LIFTOFF OF a-Si:H SOURCE / DRAIN METAL:

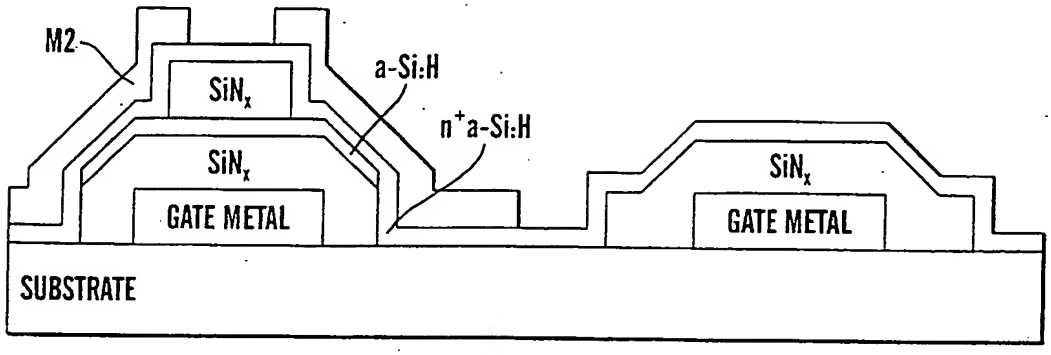

Fig.4l

ETCHING OF n^+LAYER:

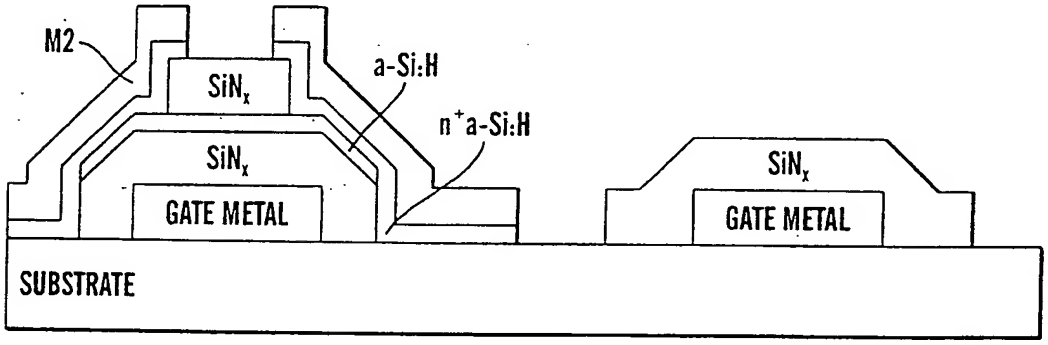

Fig.4m

PATTERING OF PHOTORESIST FOR LIFTOFF OF ORGANIC TFT METALLIZATION (MASK V):

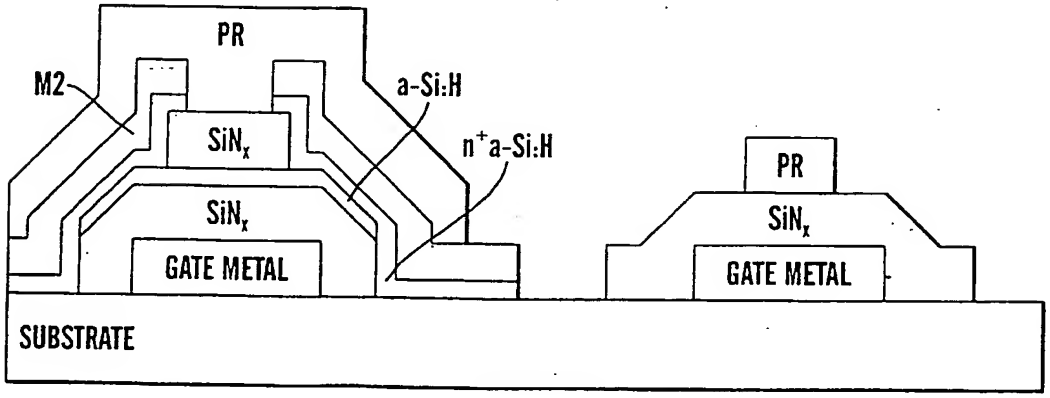

Fig.4n

DEPOSITION OF TOP METALLIZATION:

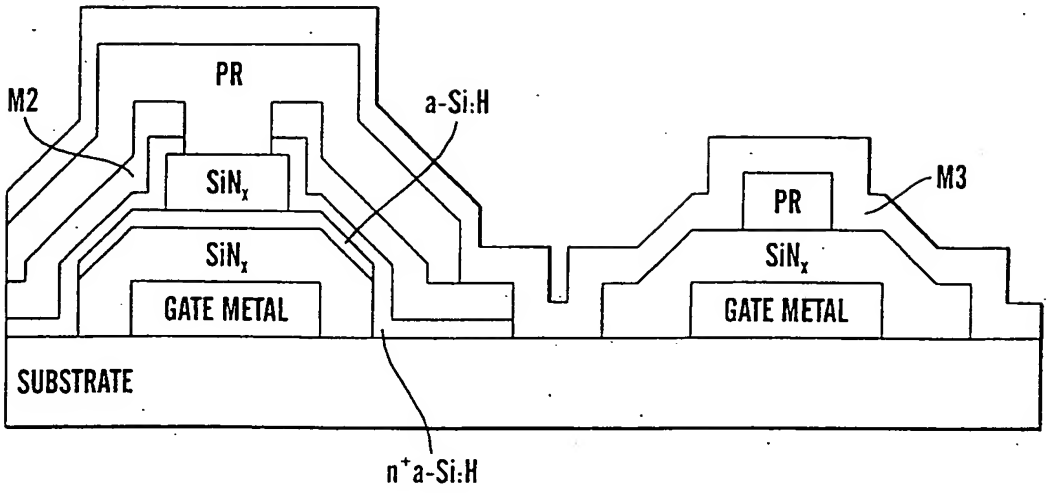

Fig.4o

LIFTOFF OF TOP METALLIZATION:

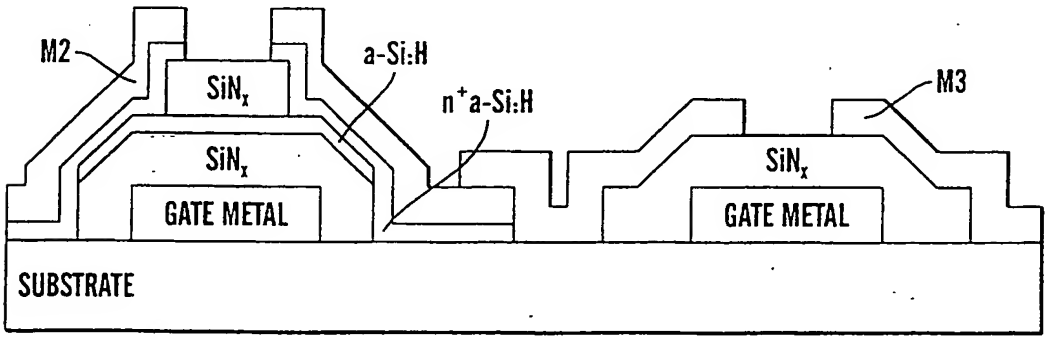

Fig.4p

DOUBLE LAYER LITHOGRAPHY FOR ISOLATION:

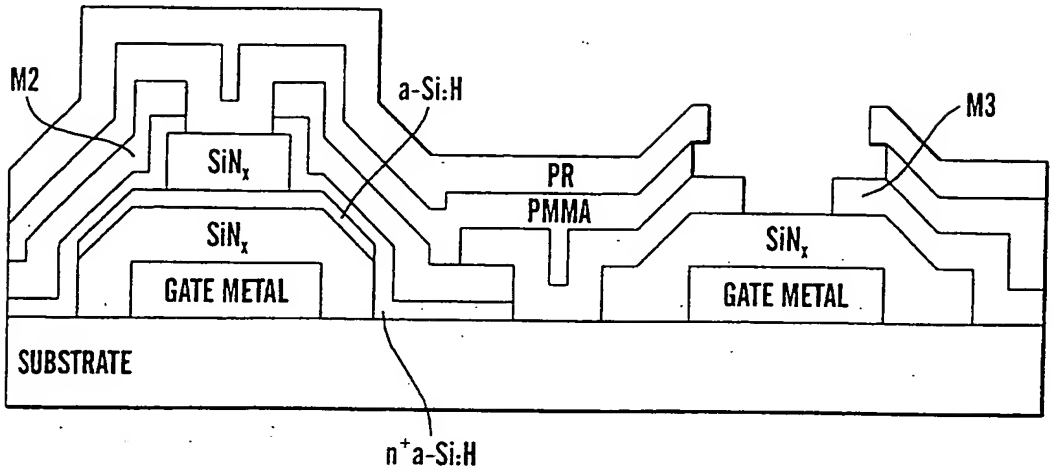

Fig.4q

DEPOSITION OF PENTACENE ORGANIC SEMICONDUCTOR:

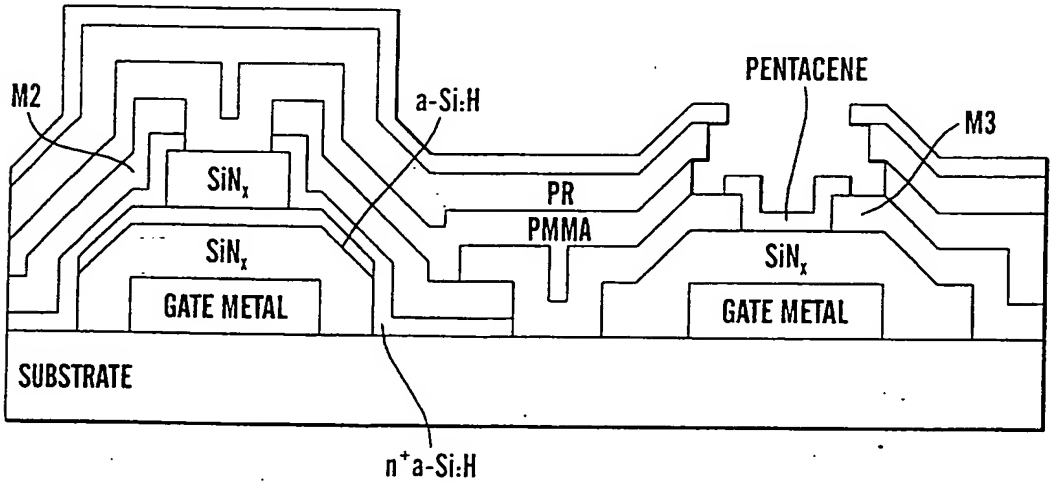

Fig.4r

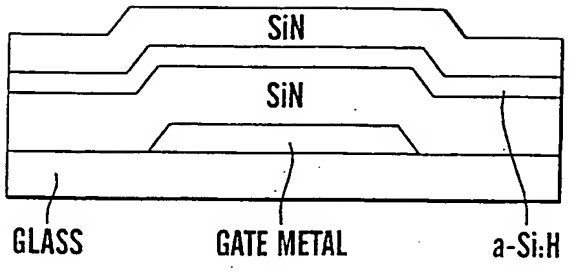

Fig.5a

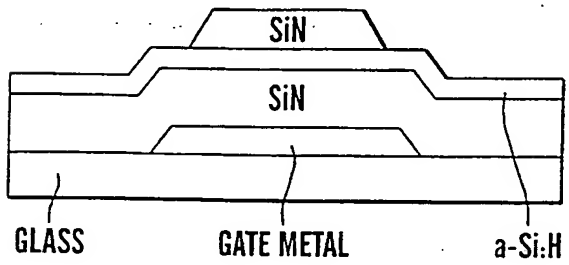

Fig.5b

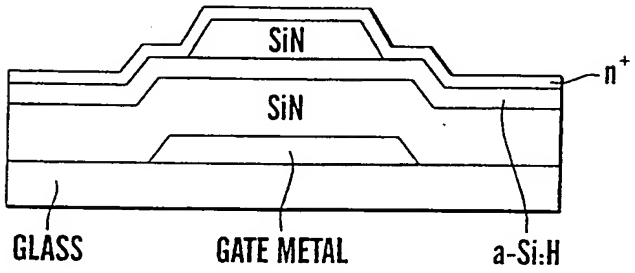

Fig.5c

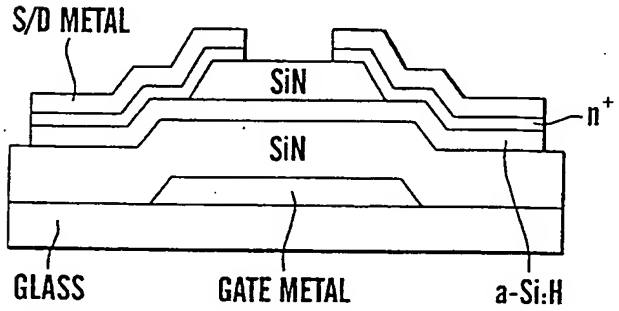

Fig.5d

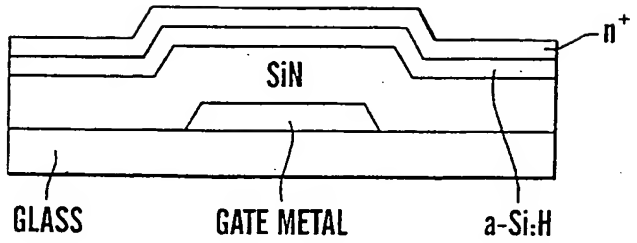

Fig.6a

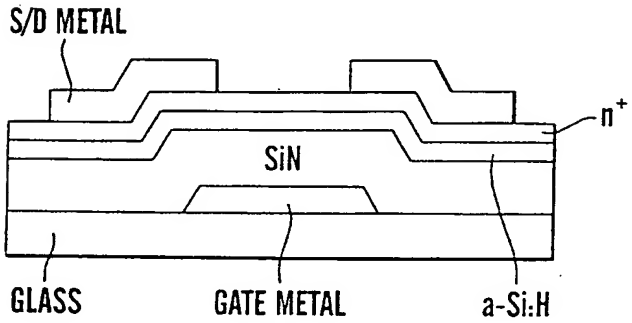

Fig.6b

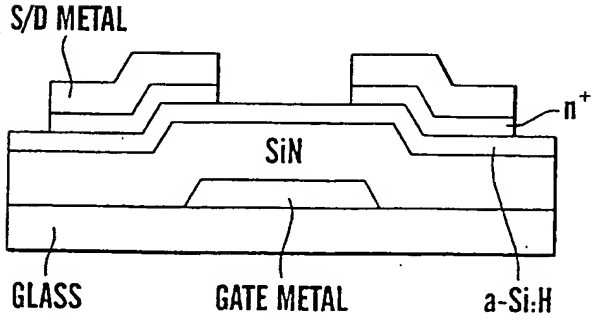

Fig.6c

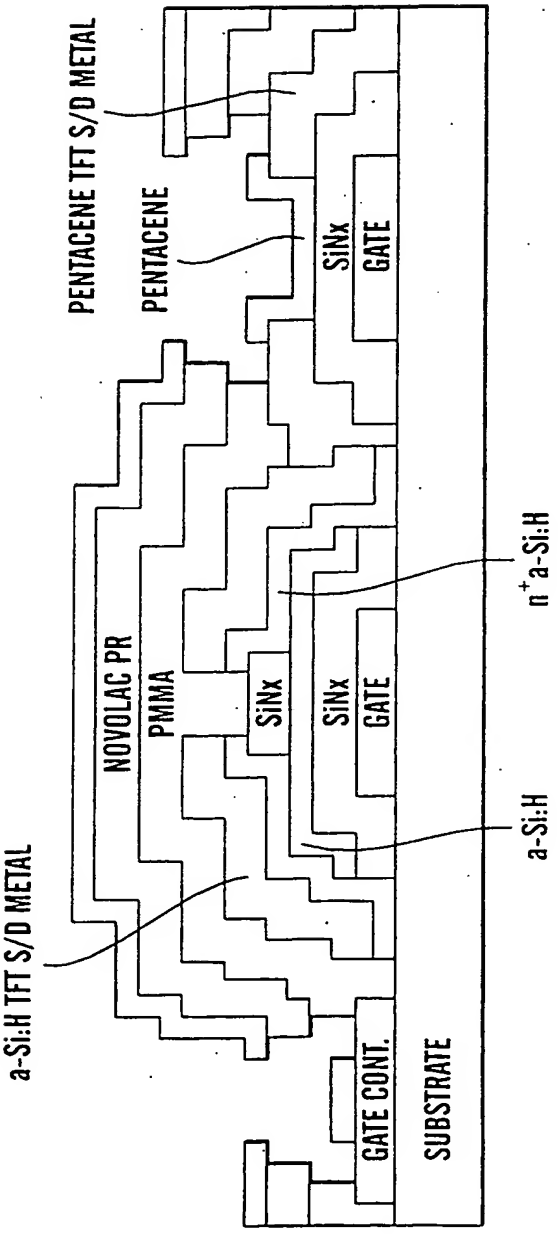
PENTACENE TFT S/D METAL
PENTACENE
SiNx
GATE
n+a-Si:H
NOVOLAC PR
PMMA
SiNx
SiNx
GATE
a-Si:H
a-Si:H TFT S/D METAL
GATE CONT.
SUBSTRATE

Fig.7a

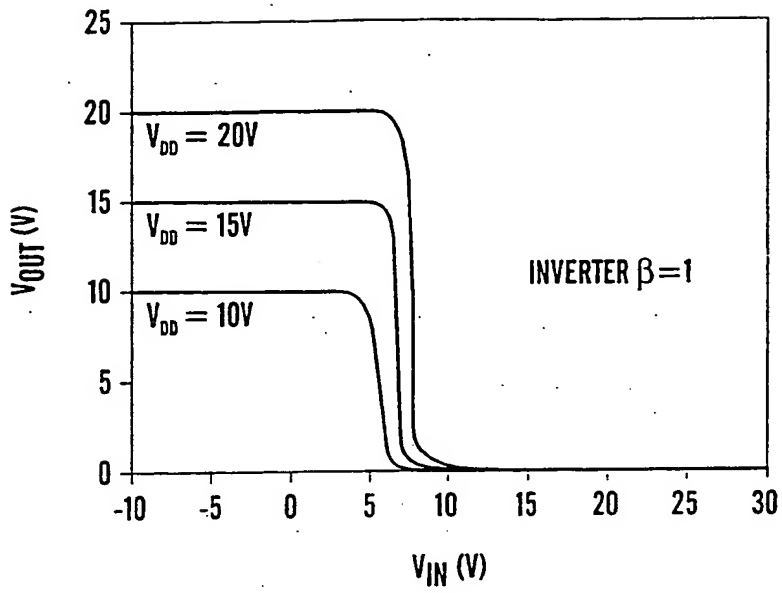

Fig.8a

VOLTAGE TRANSFER CURVE OF a-Si:H / PENTACENE INVERTER

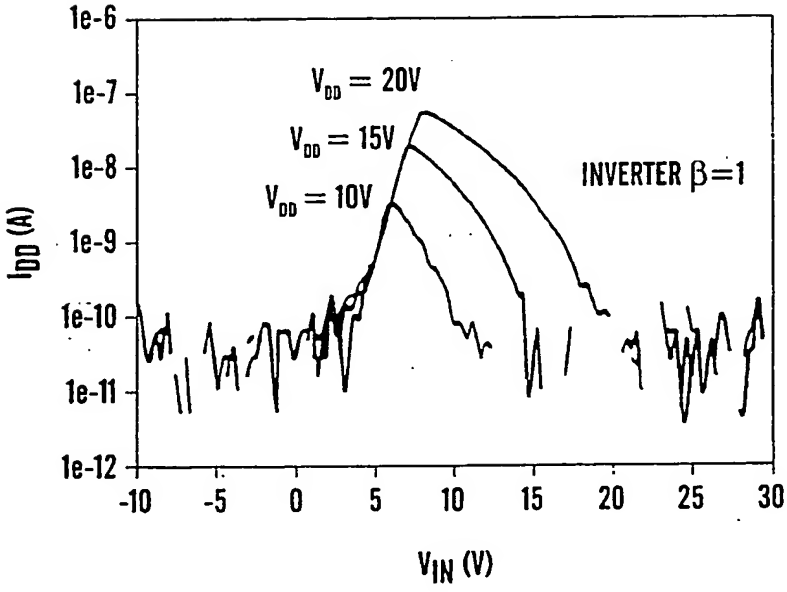

Fig.8b

TRANSIENT CURRENT OF a-Si:H / PENTACENE INVERTER

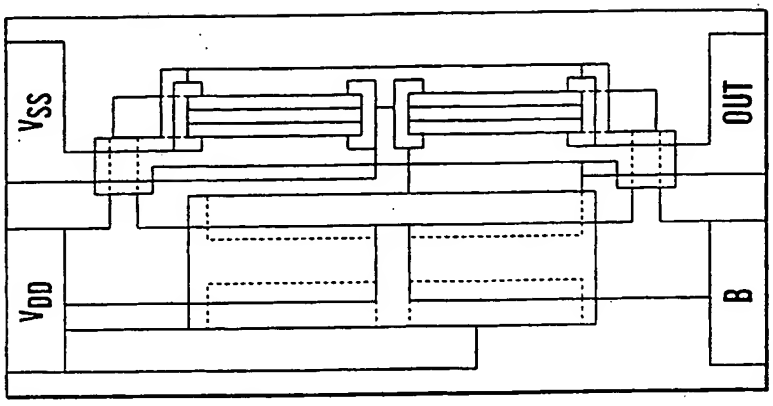

Fig.9a

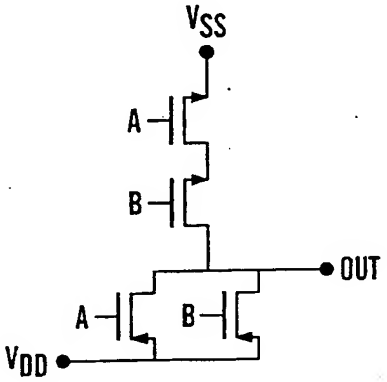

Fig.9b

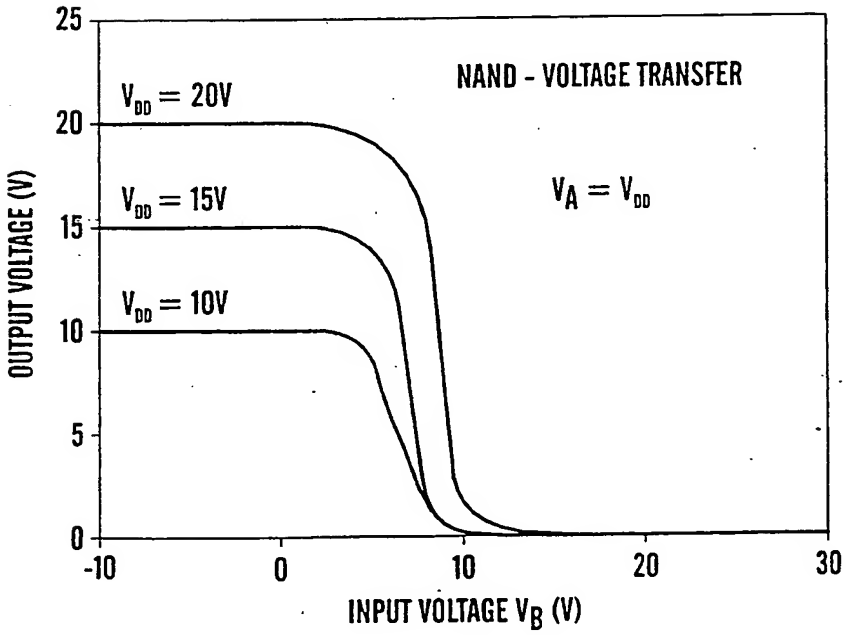

Fig.9c

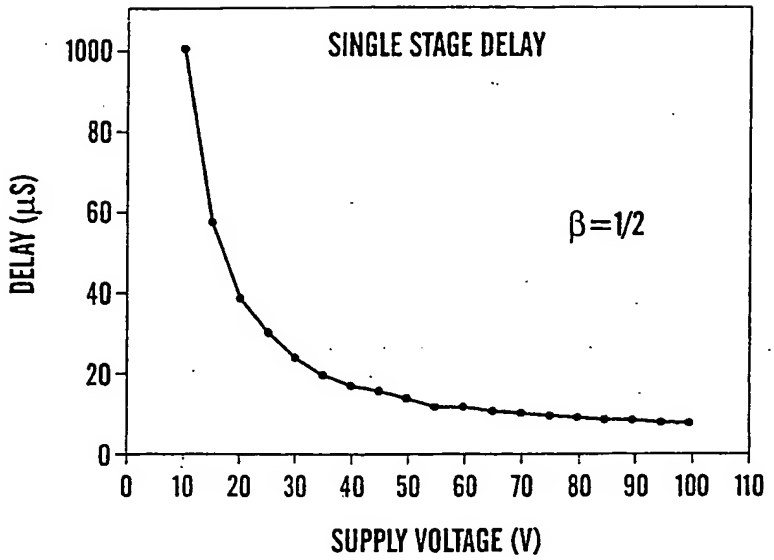

Fig. 12a

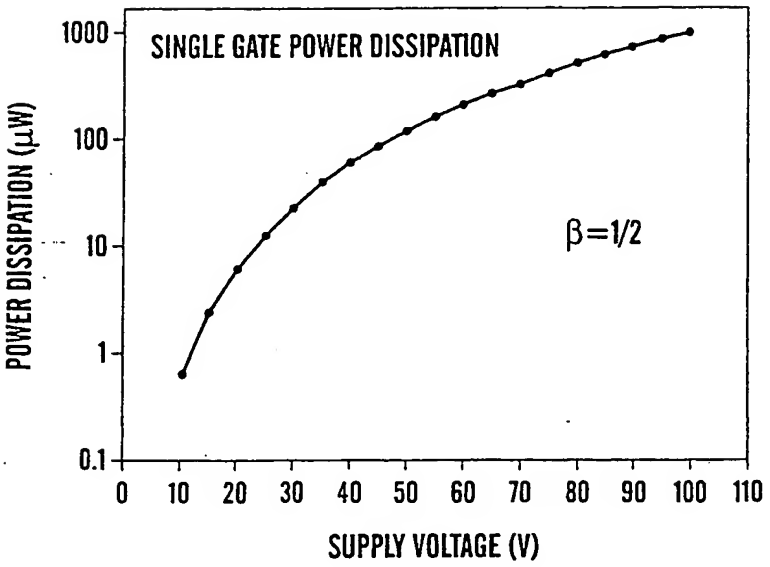

Fig. 12b

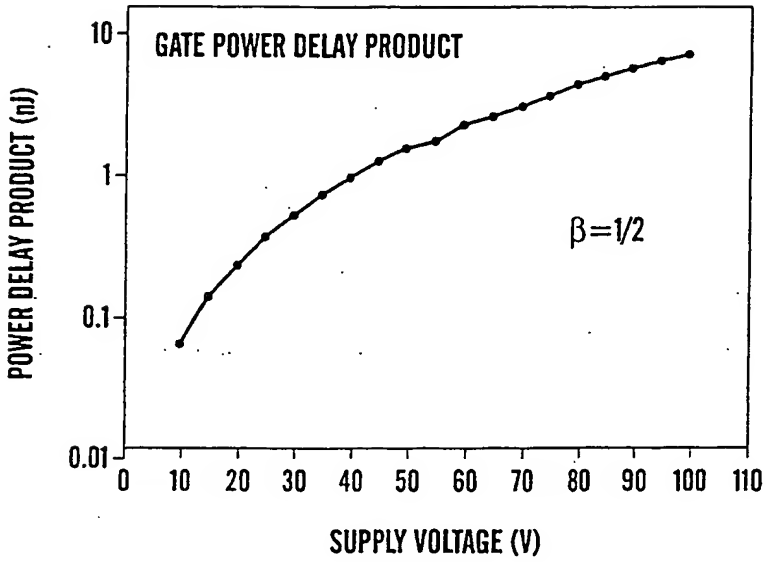

Fig.12c

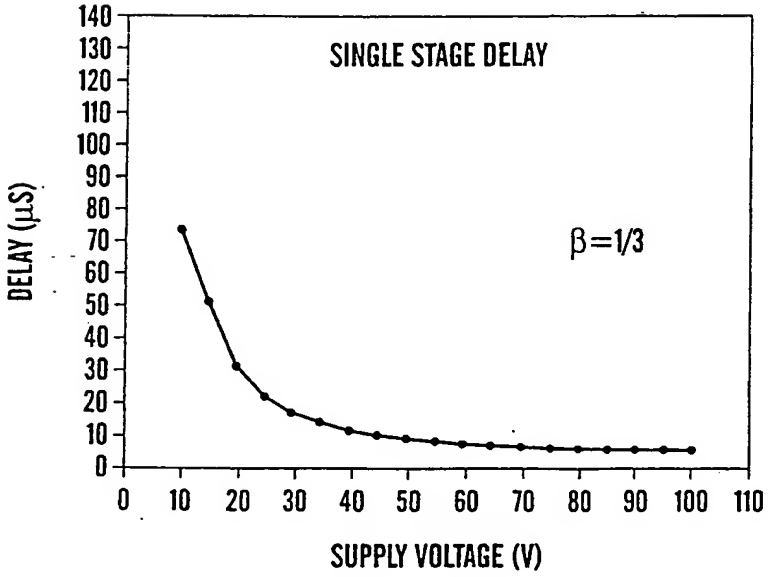

Fig.13a

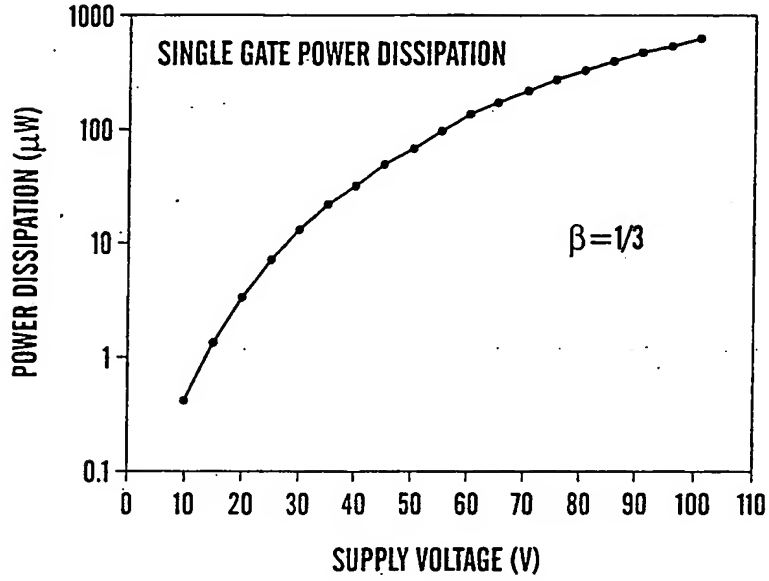

Fig. 13b

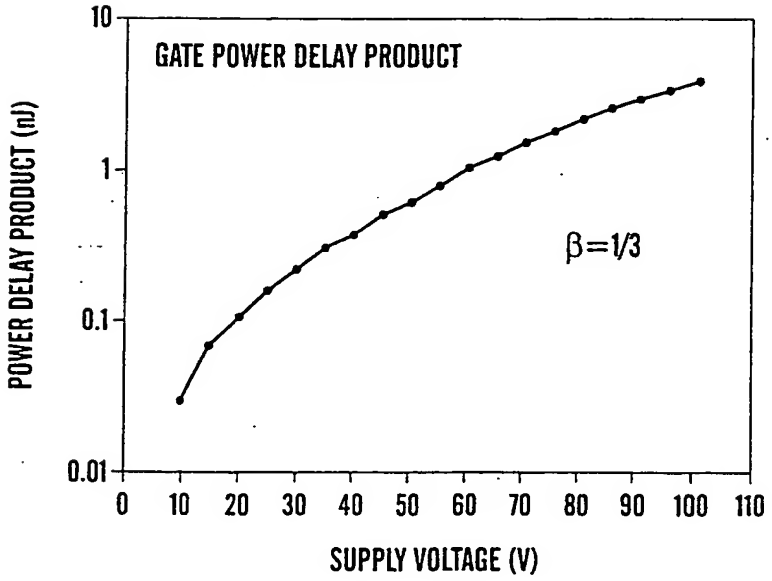

Fig. 13c

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